

8		7		6		5		4		3		2		1	
D	DESIGN		DESCRIPTION		SCHEMATIC		BOARD		MCO		PANEL		D		
	J213/MLB_COFFEE		POR CFL MLB		051-04273		820-01598		056-07680-16		057-01595				
	J213/FLEX_AUDIOJACK		AUDIO JACK, AMR, AND MESA		051-04122		821-02091		056-07548-15		N/A				
	J680/FLEX_USBC		LEFT SIDE USB TONGUE FLEX		051-03140		821-01646		056-05483-A		N/A				
	J132/FLEX_BMU_SIGNAL		SIGNALS TO BMU		051-03342		821-01726		056-05589-A		N/A				
	J79/FLEX_BMU_PWR		POWER TO/FROM BMU		051-00927		821-00447		056-02301-A		N/A				
	J130/FLEX_TCON_MLB		DISPLAYPORT FROM MLB TO TCON		051-01199		821-00586		056-02785-07		N/A				
	J213/FLEX_TRACKPAD		MLB TO TRACKPAD		051-04335		821-02218		056-07655-05		N/A				
	J130/FLEX_KB_3D		KB FLEX FOR ALL 3 KB TYPES		051-02011		821-01046		056-03725-B		N/A				
	J213/FLEX_3MIC		MIC FLEX		051-04441		821-02265		056-07754-17		N/A				
B	J79/GRAPE_FLEX		DFR TOUCH FLEX		051-01338		821-00681		056-02220-A		N/A		B		
	DFR DAUGHTER FLEX		DFR DAUGHTER FLEX		VENDOR		VENDOR		099-14398		N/A				
	J213/DEV_MLB_COUPON		IMPEDENCE COUPON		951-08932		920-06560		998-16565-01		057-01595				
8		7		6		5		4		3		2		1	

Apple Inc.

051-04273

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svt-1

2 OF 500


2 OF 98

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SYSTEM PCB SUMMARY

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SYSTEM PCB SUMMARY

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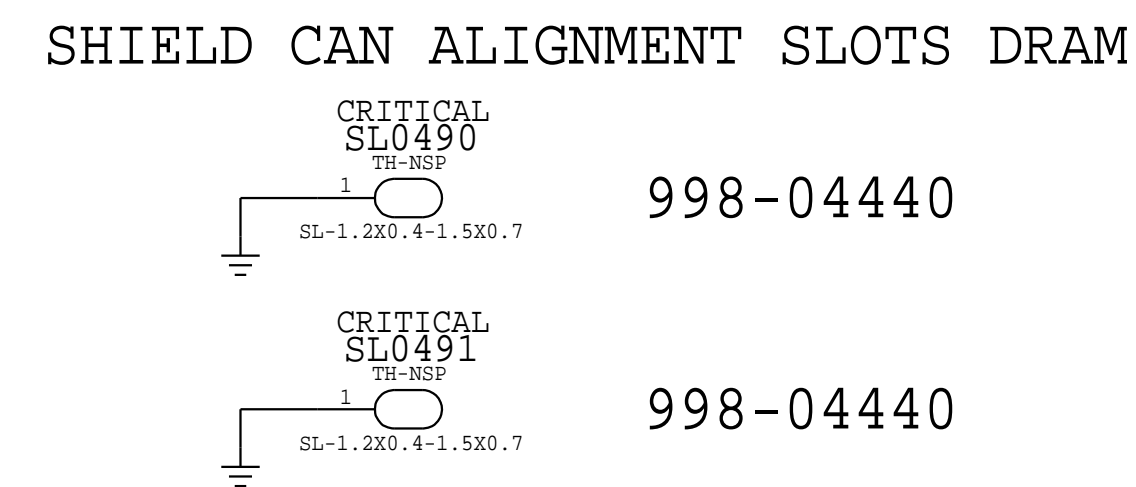
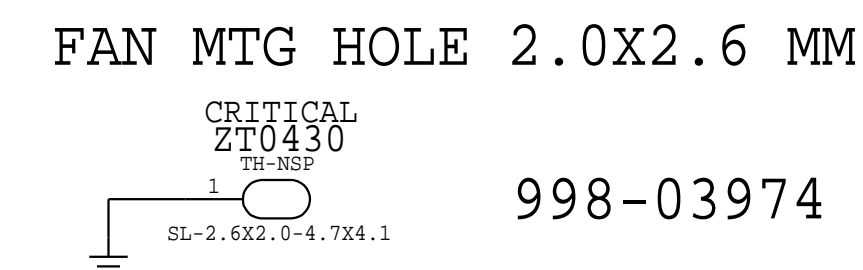
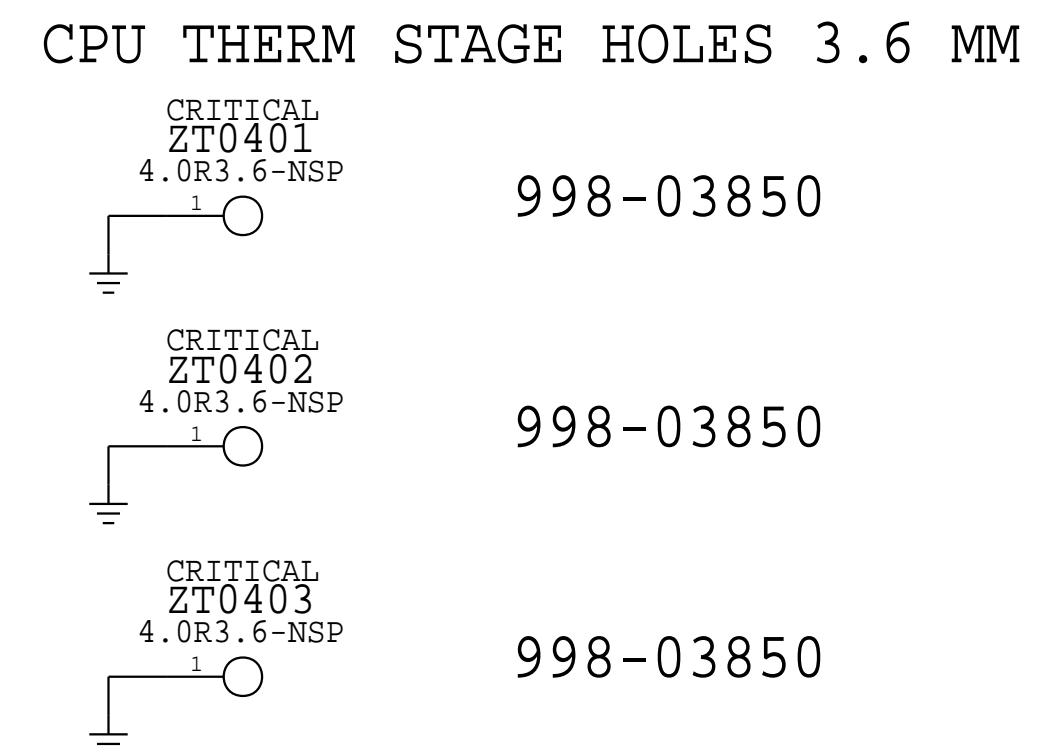
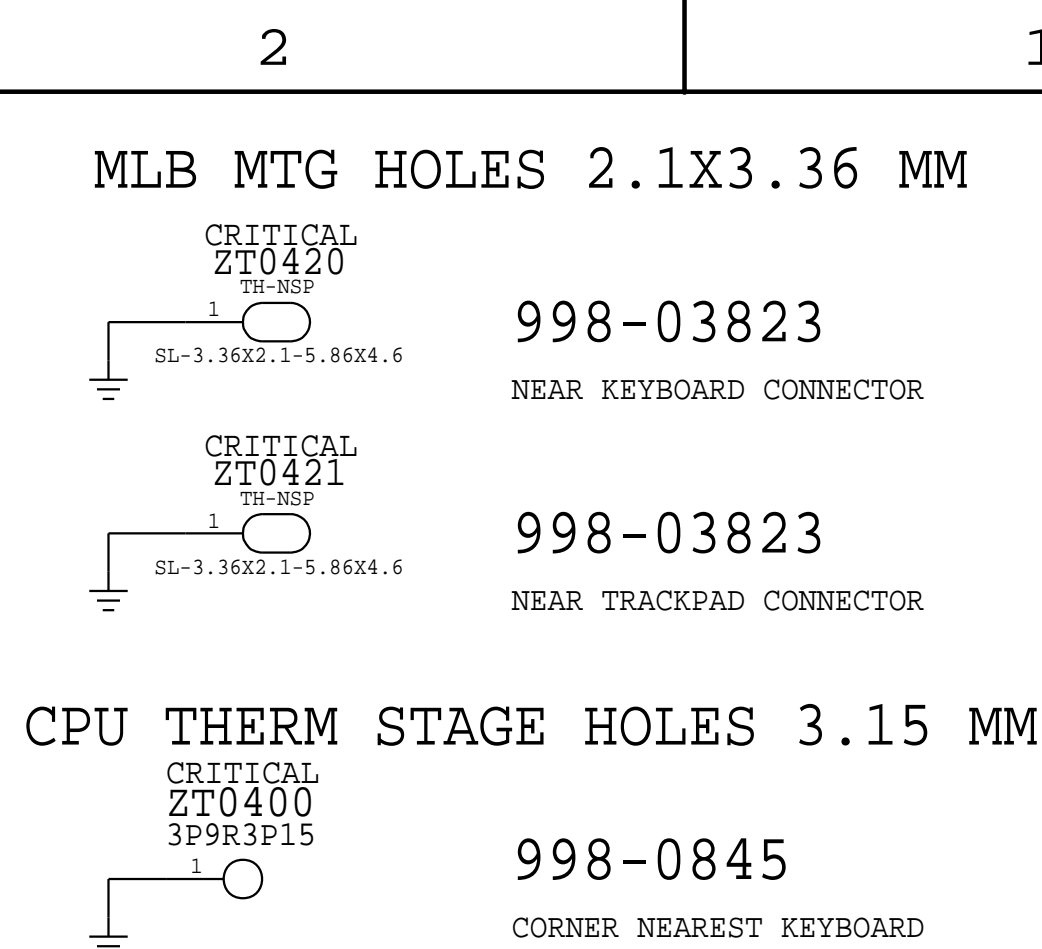
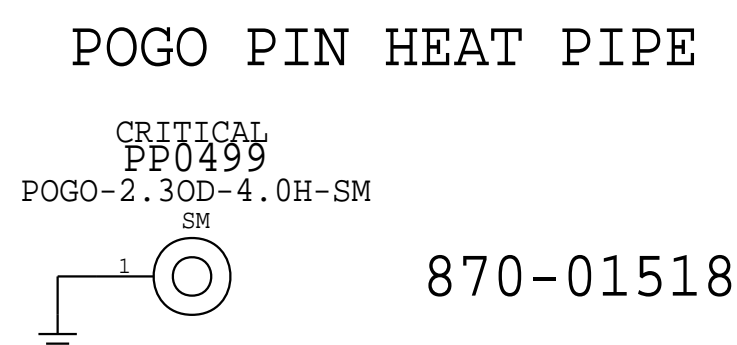
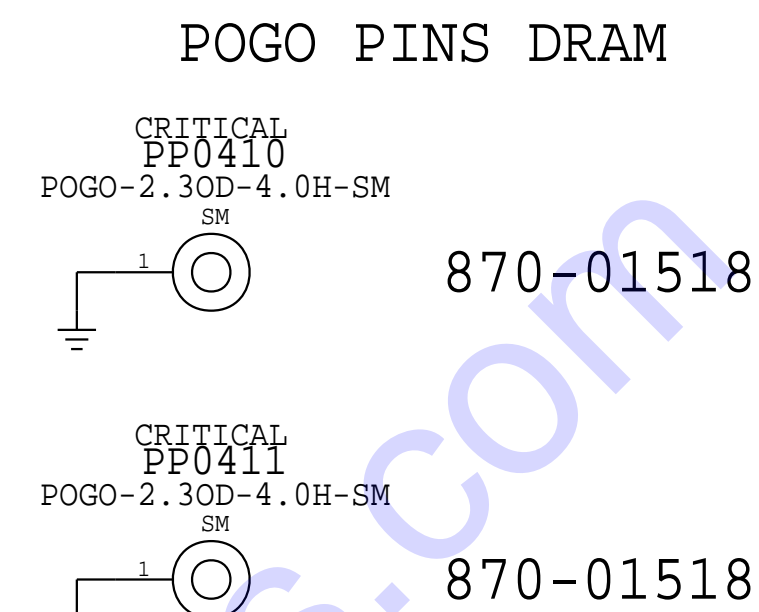
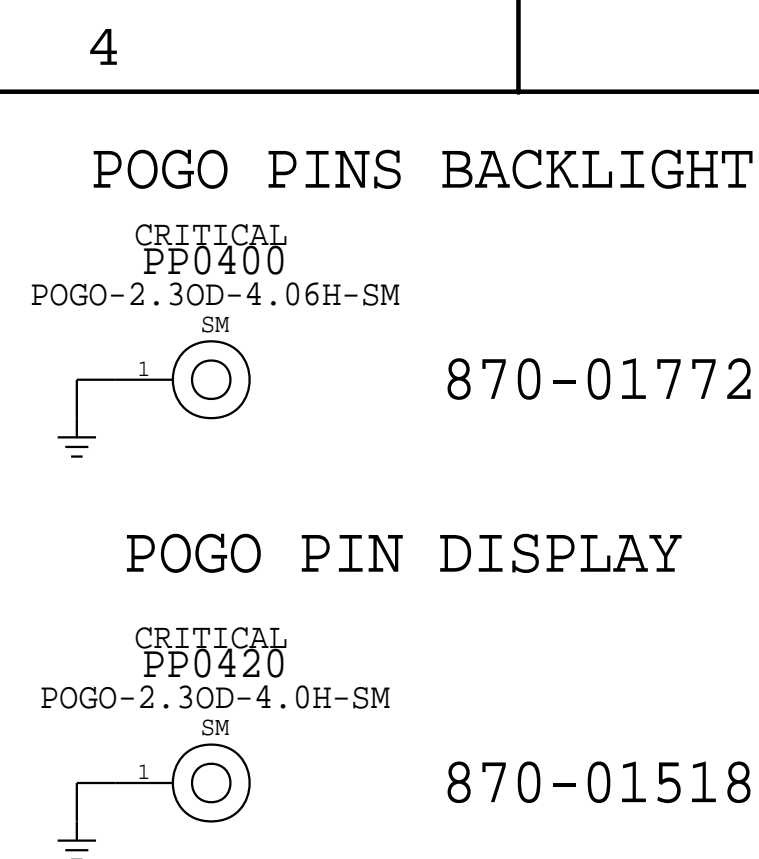
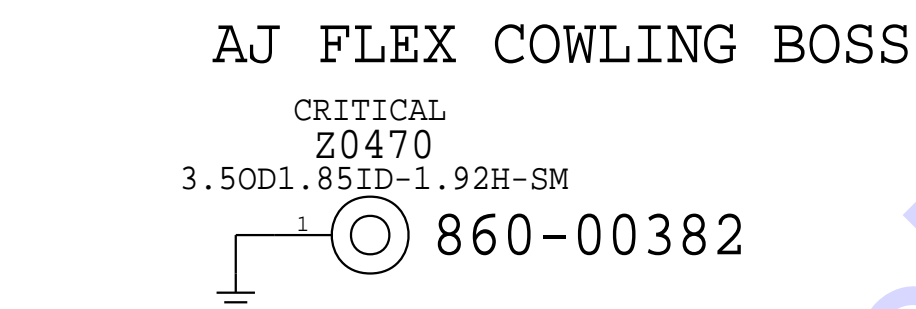
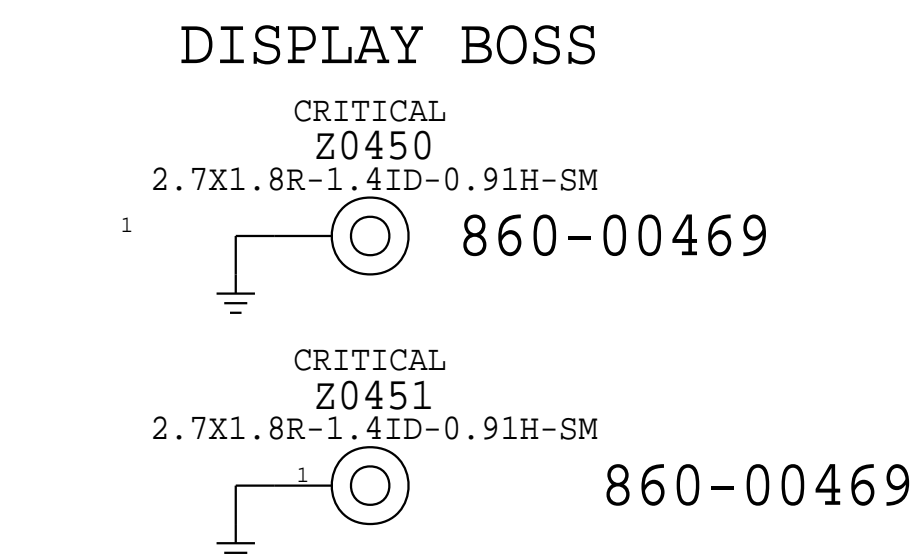
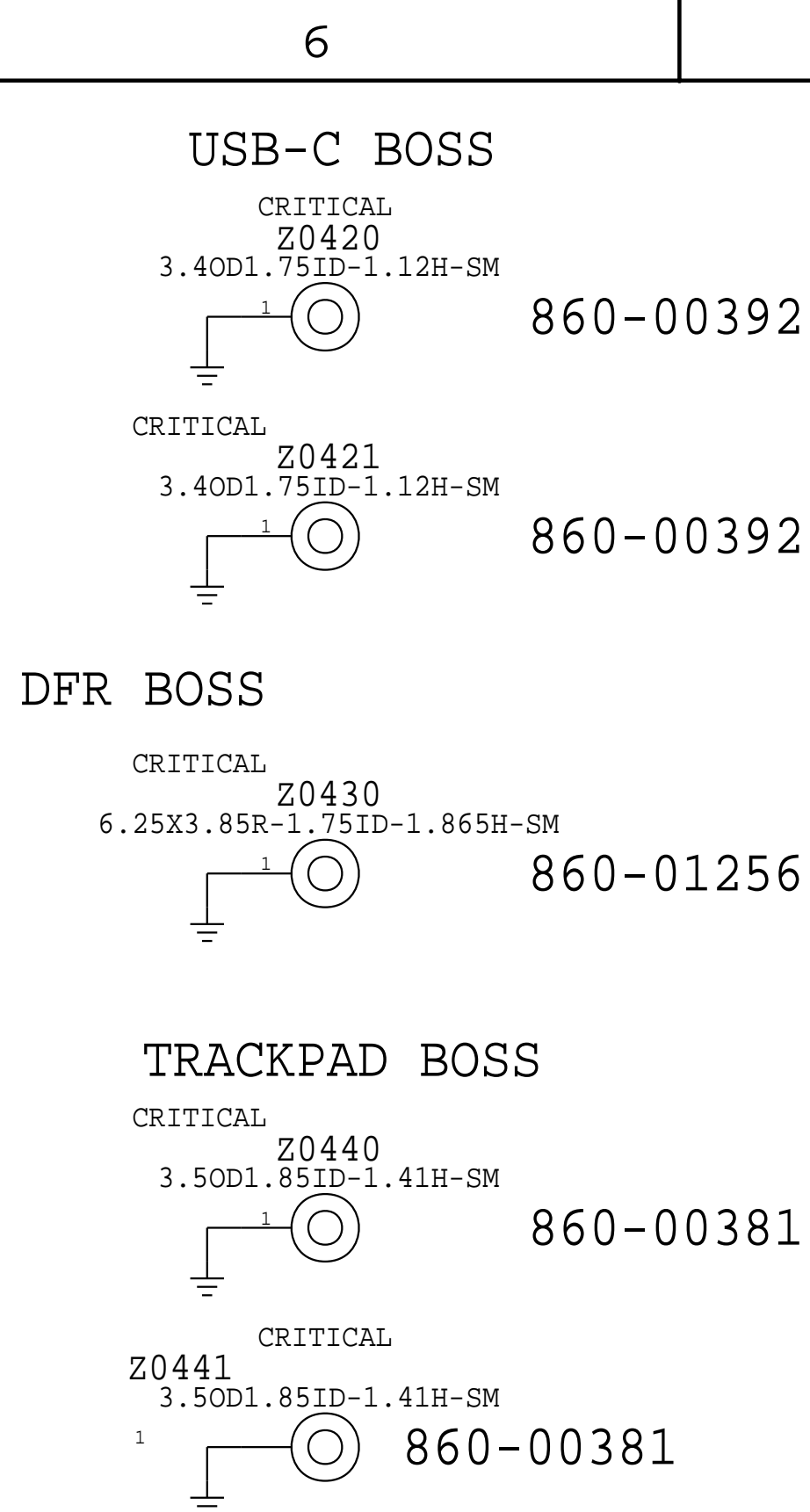
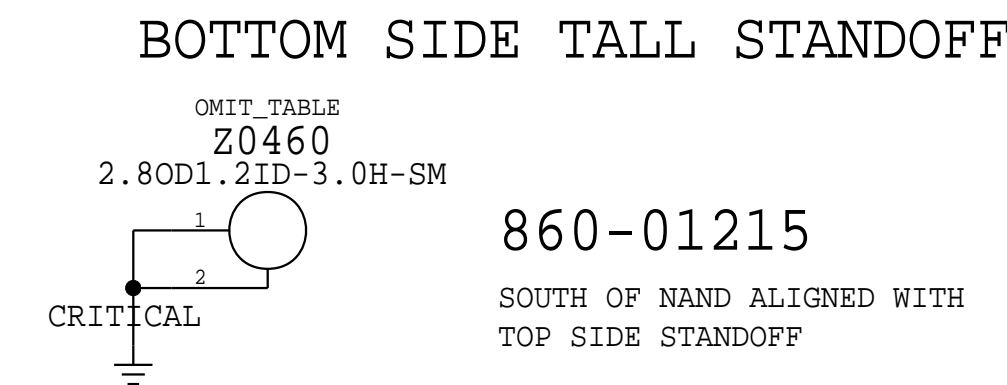
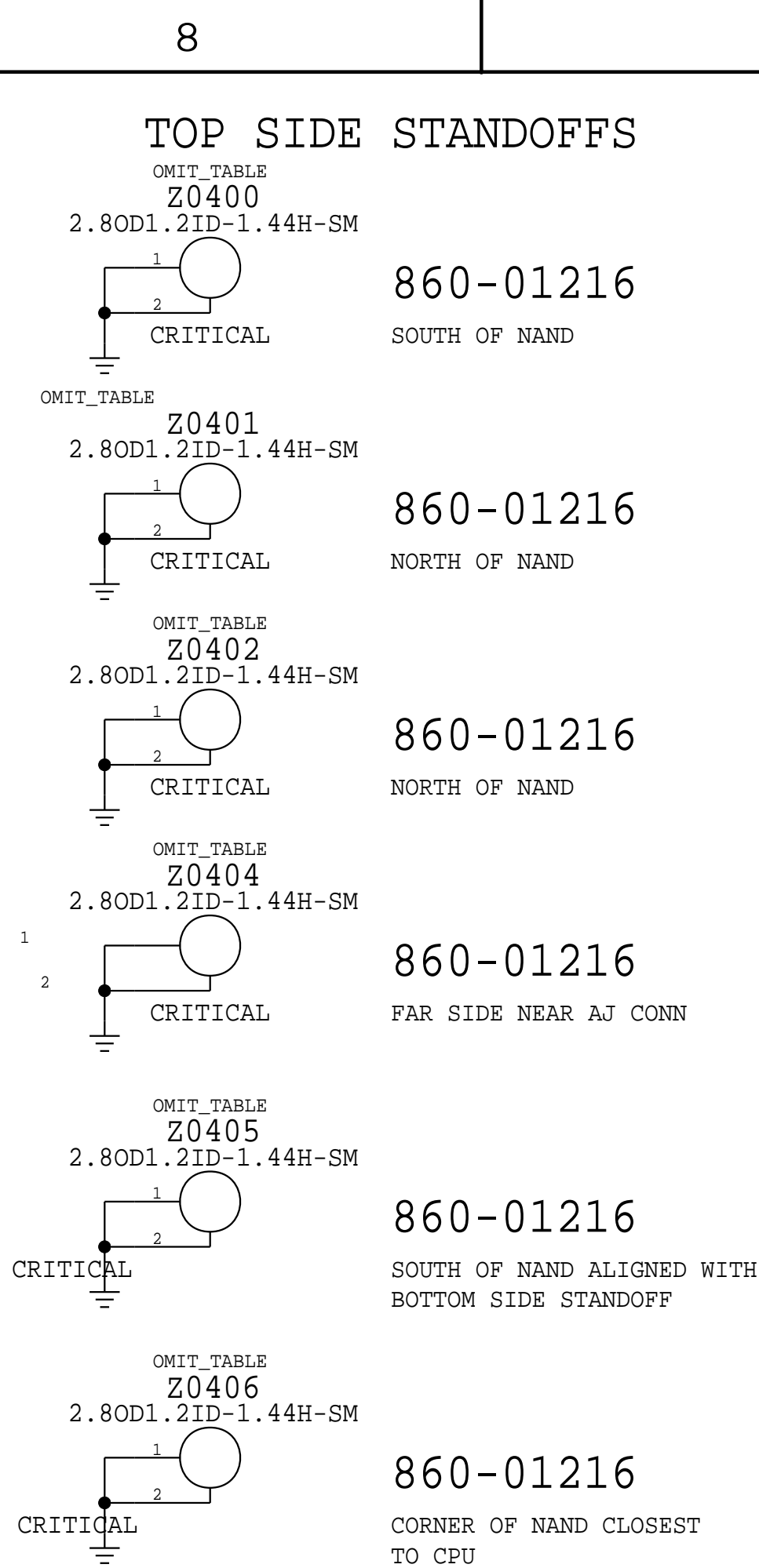
evt-1

PAGE

2 OF 500

SHEET

2 OF 98



2X PLATED SLOTS IN MEM AREA DUE TO
SPACE CONSTRAINTS <RDAR:///44382678>
ALL OTHER SHIELD ALIGNMENT SLOTS ARE
NPTH + GND RING FOR BETTER TOLERANCE

USB-C SHIELD

806-19049	1	SHIELD CAN,HOLES,TITAN RIDGE,X1533	USBC_CAN	CRITICAL	USBC_CAN
870-07967	1	TAPE,COND,TITANRIDGE,CAN,X1533	USBC_CAN_TAPE	CRITICAL	USBC_CAN_TAPE
806-18559	1	FENCE,TITAN RIDGE,X1533	USBC_FENCE	CRITICAL	USBC_FENCE
870-07841	1	TAPE,COND,TITANRIDGE,MLB,BTM,X1533	USBC_FENCE_TAPE	CRITICAL	USBC_FENCE_TAPE

MEGA SHIELD

806-19050	1	SHIELD CAN,HOLES,MEGA,X1533	MEGA_CAN	CRITICAL	MEGA_CAN
870-07968	1	TAPE,COND,MEGA,CAN,X1533	MEGA_CAN_TAPE	CRITICAL	MEGA_CAN_TAPE
806-18561	1	FENCE,MEGA,X1533	MEGA_FENCE	CRITICAL	MEGA_FENCE
870-07842	1	TAPE,COND,MEGA,MLB,BTM,X1533	MEGA_FENCE_TAPE	CRITICAL	MEGA_FENCE_TAPE

DRAM SHIELD TOP

806-19048	1	SHIELD CAN, HOLES, DRAM, UNIV, X1533	DRAM_TOP_CAN	CRITICAL	DRAM_TOP_CAN
870-07966	1	TAPE, COND, DRAM, CAN, X1533	DRAM_TOP_CAN_TAPE	CRITICAL	DRAM_TOP_CAN_TAPE
806-18560	1	FENCE, DRAM, UNIV, X1533	DRAM_TOP_FENCE	CRITICAL	DRAM_TOP_FENCE
870-07840	1	TAPE, COND, DRAM, UNIV, X1533	DRAM_TOP_FENCE_TAPE	CRITICAL	DRAM_TOP_FENCE_TAPE

DRAM SHIELD BOTTOM


806-19048	1	SHIELD_CAN,HOLES_DRAM,UNIV.X1533	DRAM_BOT_CAN	CRITICAL	DRAM_BOT_CAN
870-07966	1	TAPE_COND_DRAM_CAN,X1533	DRAM_BOT_CAN_TAPE	CRITICAL	DRAM_BOT_CAN_TAPE
806-18560	1	FENCE_DRAM,UNIV.X1533	DRAM_BOT_FENCE	CRITICAL	DRAM_BOT_FENCE
870-07840	1	TAPE_COND_DRAM,UNIV.X1533	DRAM_BOT_TAPE	CRITICAL	DRAM_BOT_TAPE

TOP SIDE STANDOFFS

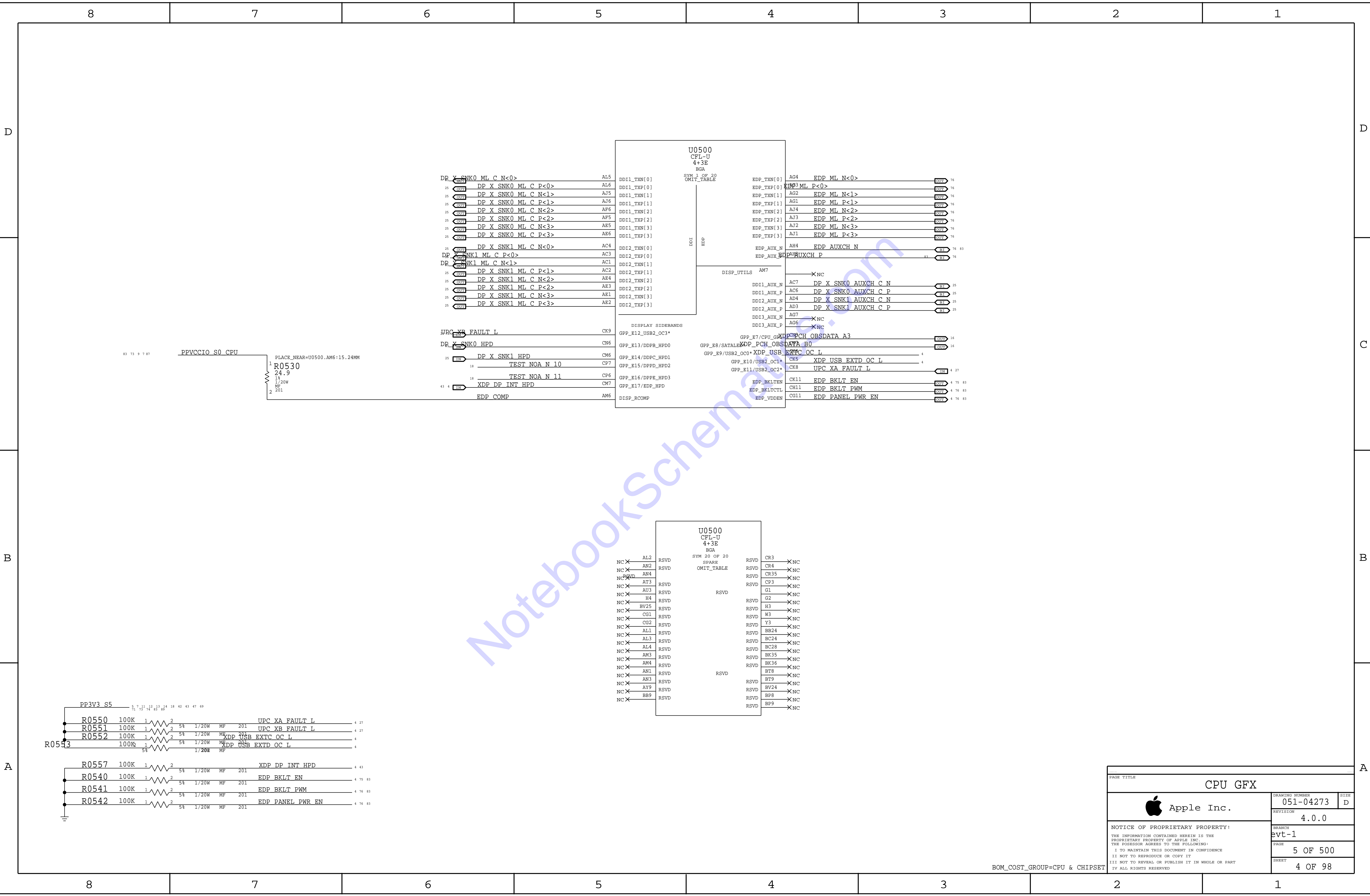
860-01216	BOSS, STANDOFF, MLB, X15320400-Z0402, Z0404-Z0406		CRITICAL	
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BOTTOM SIDE STANDOFFS

860-01215	1	BOSS,STANDOFF,MLB,TALL,X1533	Z0460	CRITICAL	
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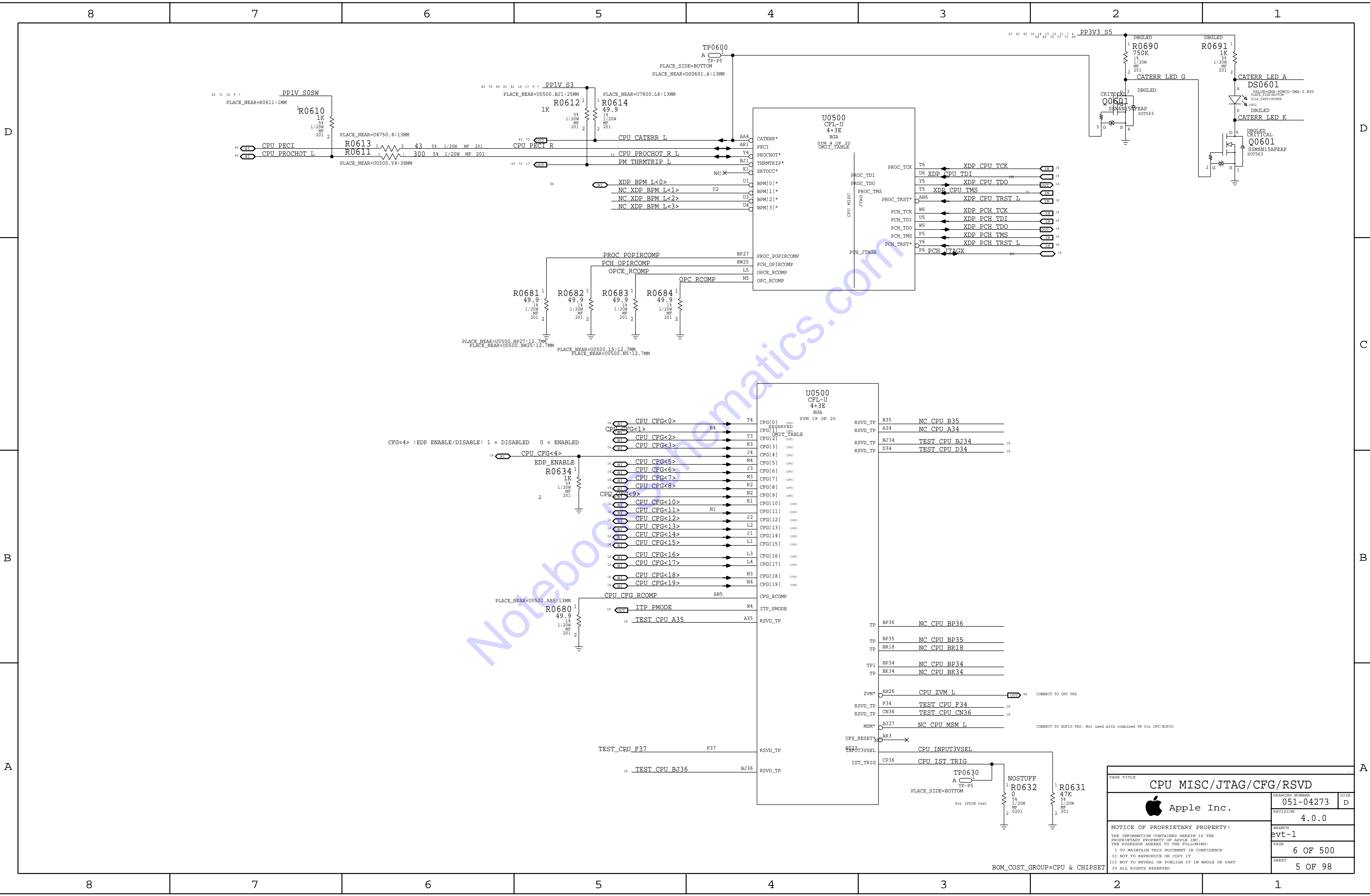
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	<div>REVISION</div> <div>4.0.0</div>		
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		<div>PAGE</div> <div>4 OF 500</div>	
		<div>SHEET</div> <div>3 OF 98</div>	

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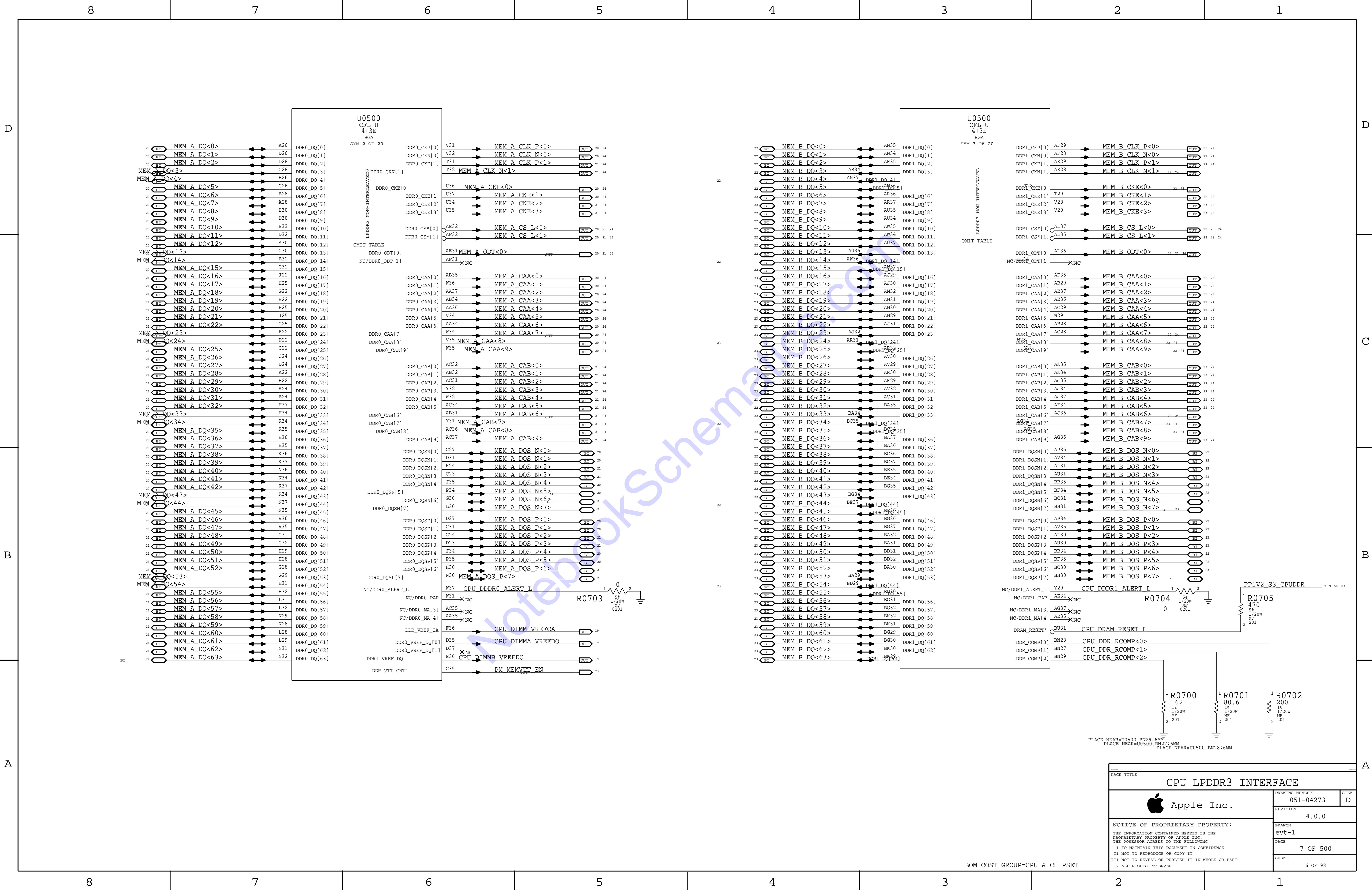



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CPU GFX		
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	PAGE	5 OF 500
	SHEET	4 OF 98

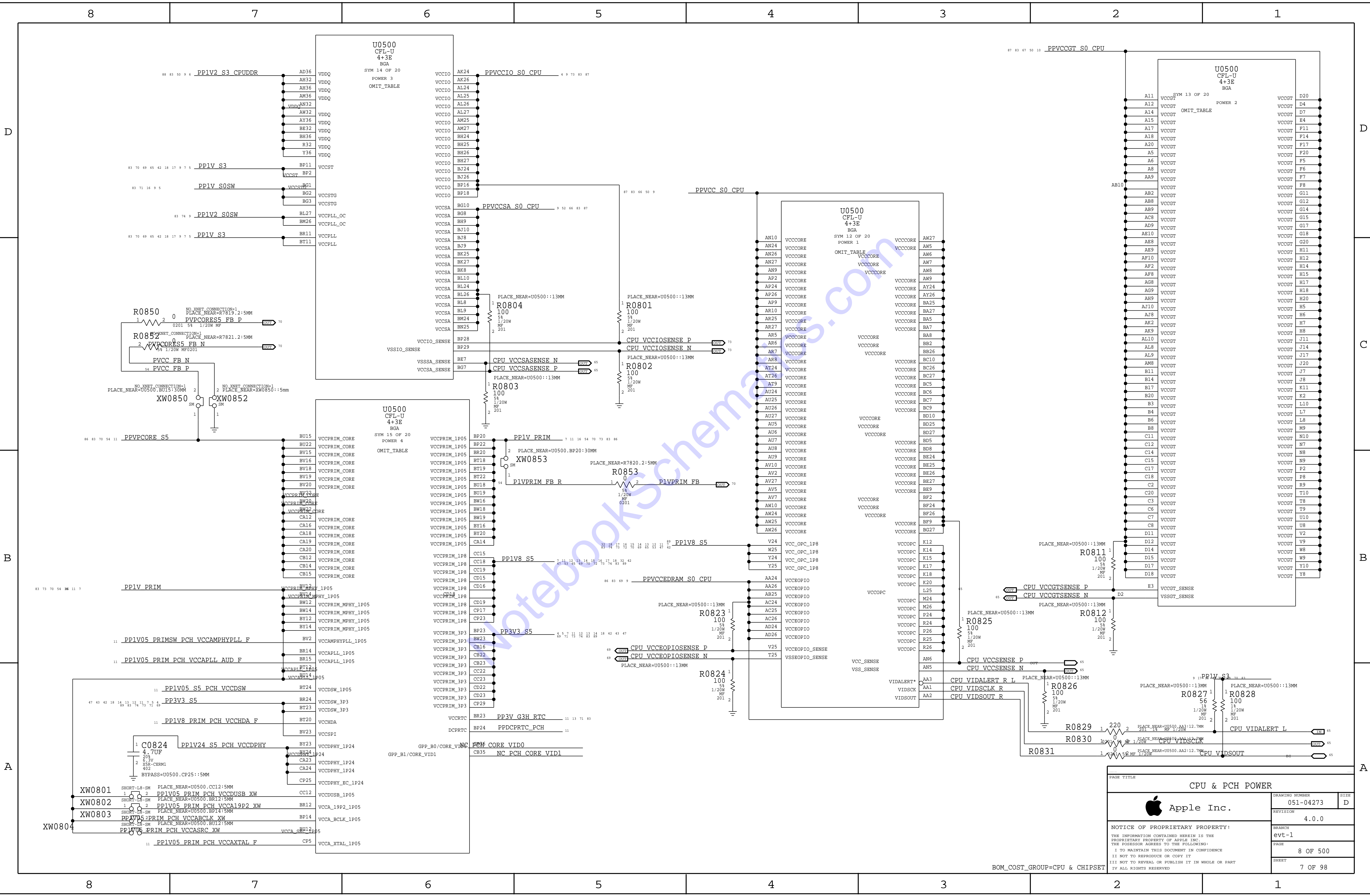
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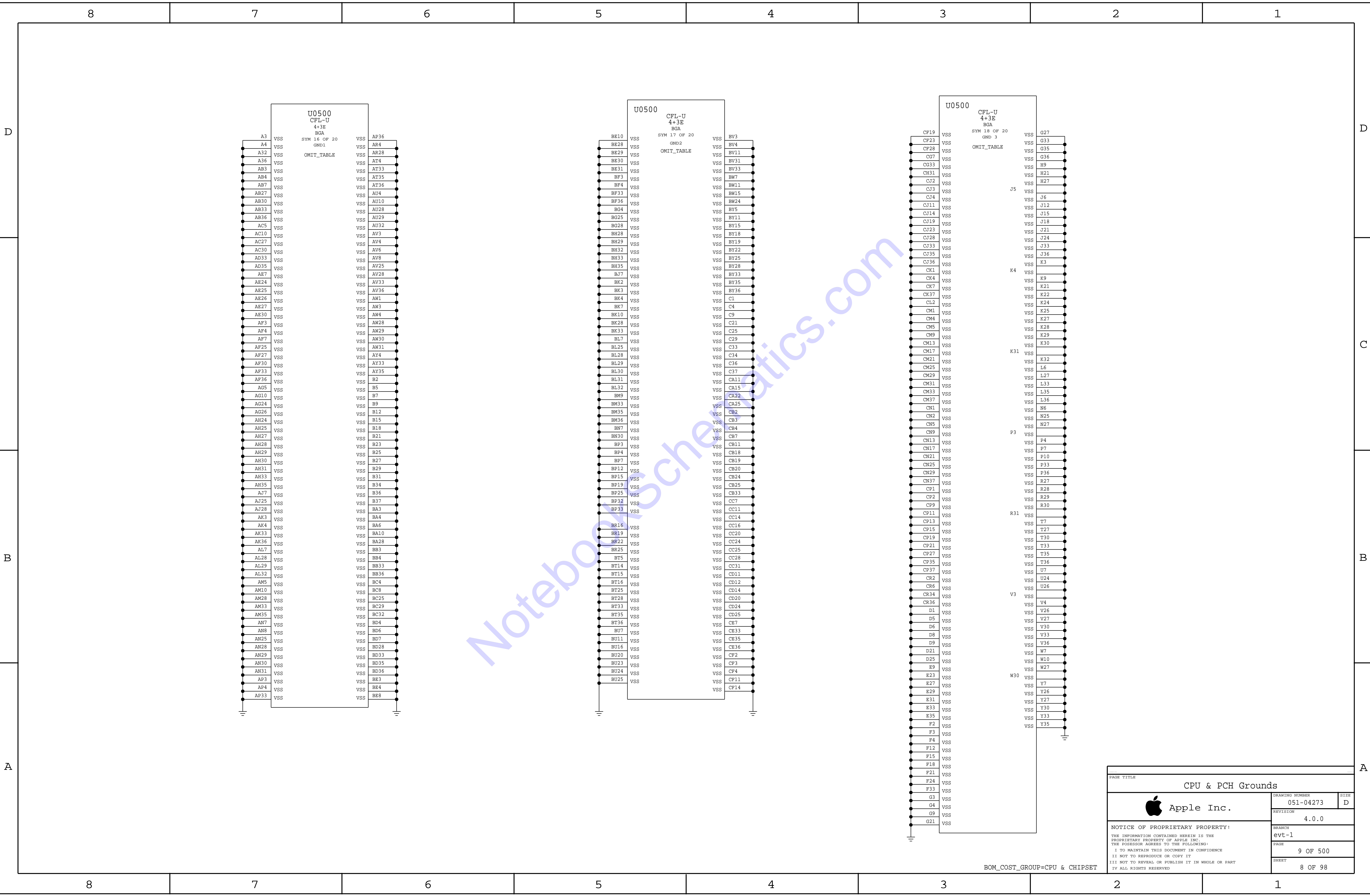
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CPU MISC/JTAG/CFG/RSVD		
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	PAGE	6 OF 500
	SHEET	5 OF 98



PAGE TITLE		
CPU LPDDR3 INTERFACE		
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	PAGE	7 OF 500
	SHEET	6 OF 98

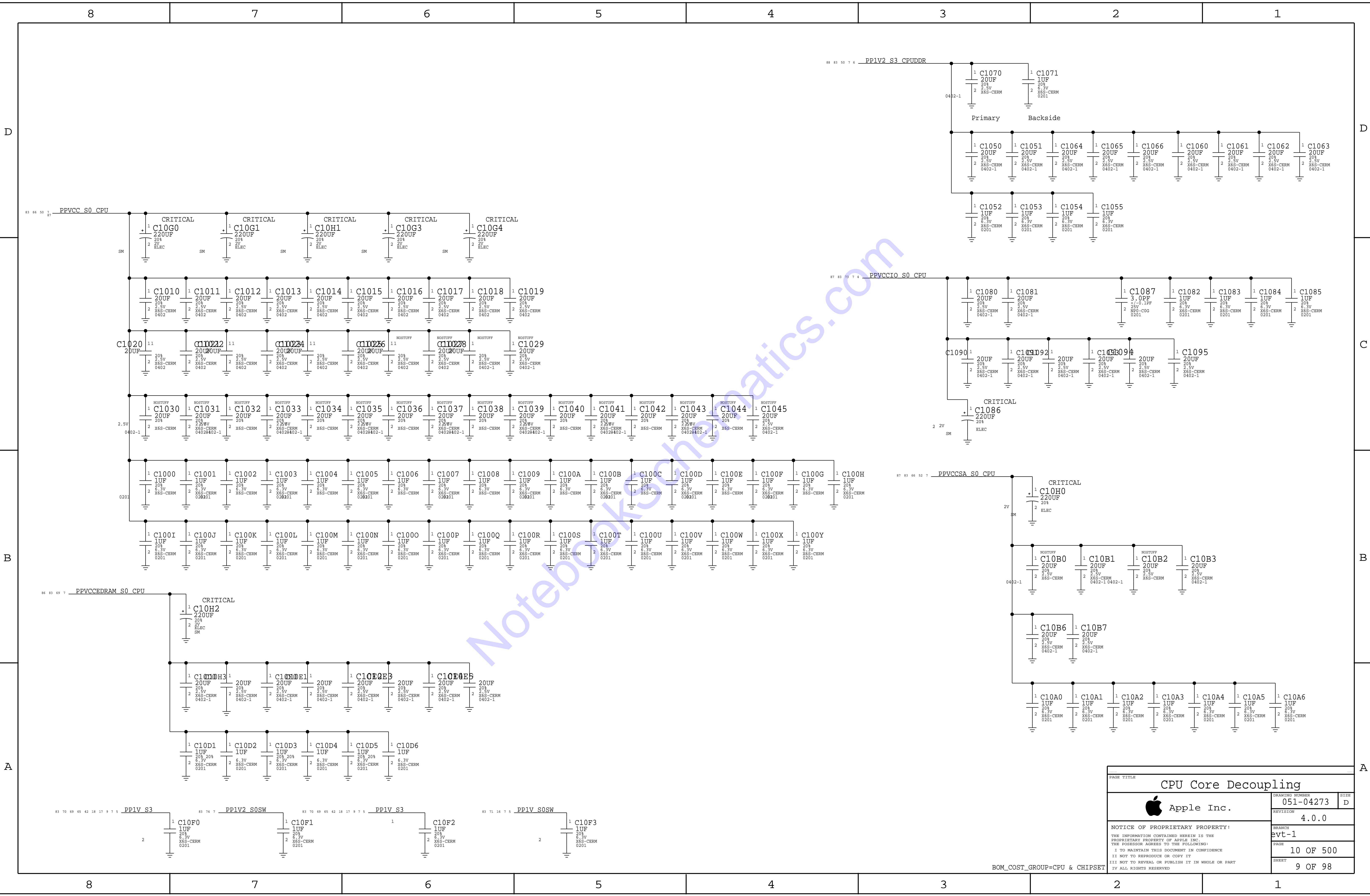



PAGE TITLE			
CPU & PCH POWER			
 Apple Inc.	DRAWING NUMBER	051-04273	SIZE
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	BRANCH	evt-1	
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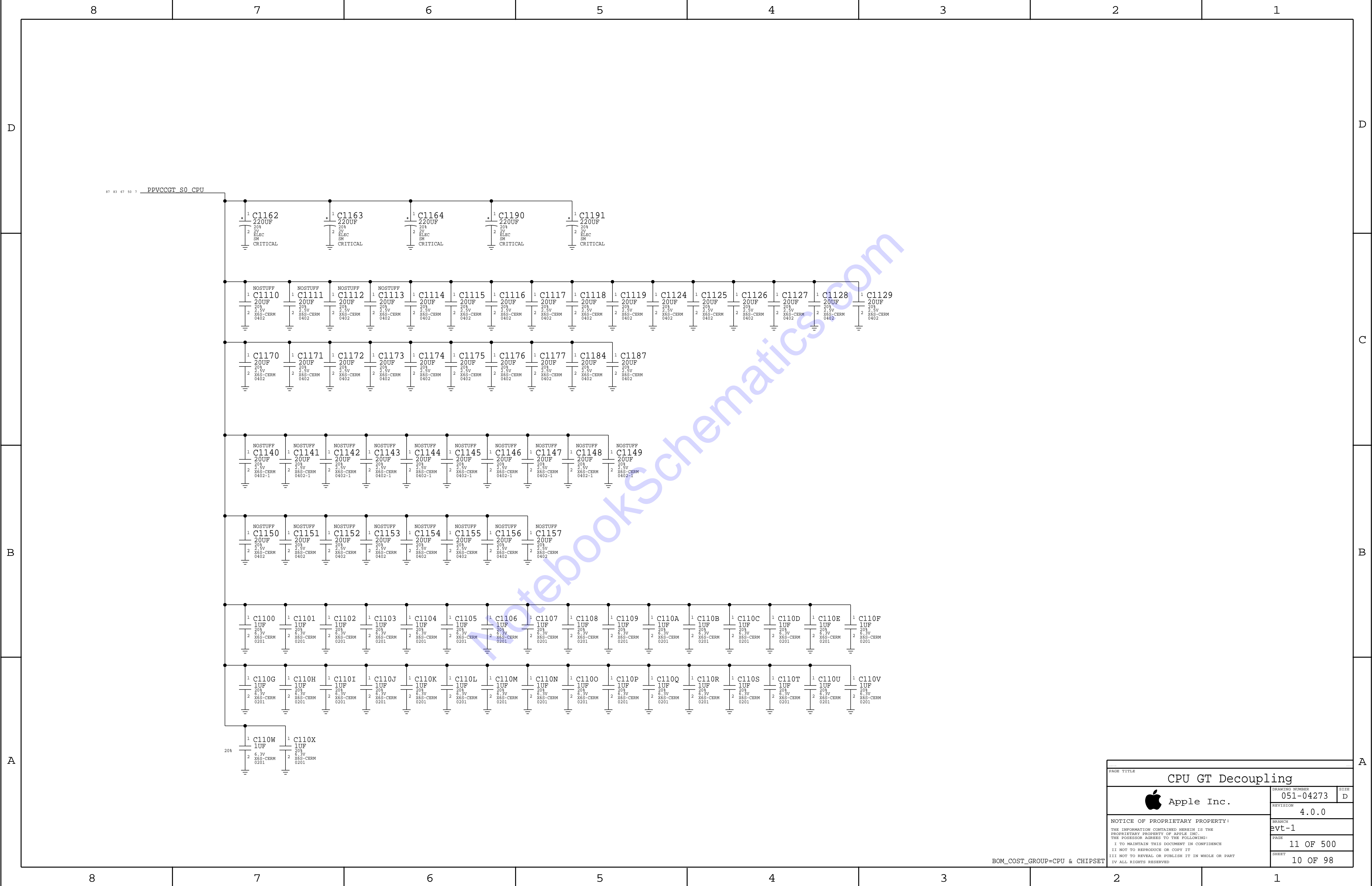



CPU & PCH Grounds		
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	PAGE	9 OF 500
	SHEET	8 OF 98

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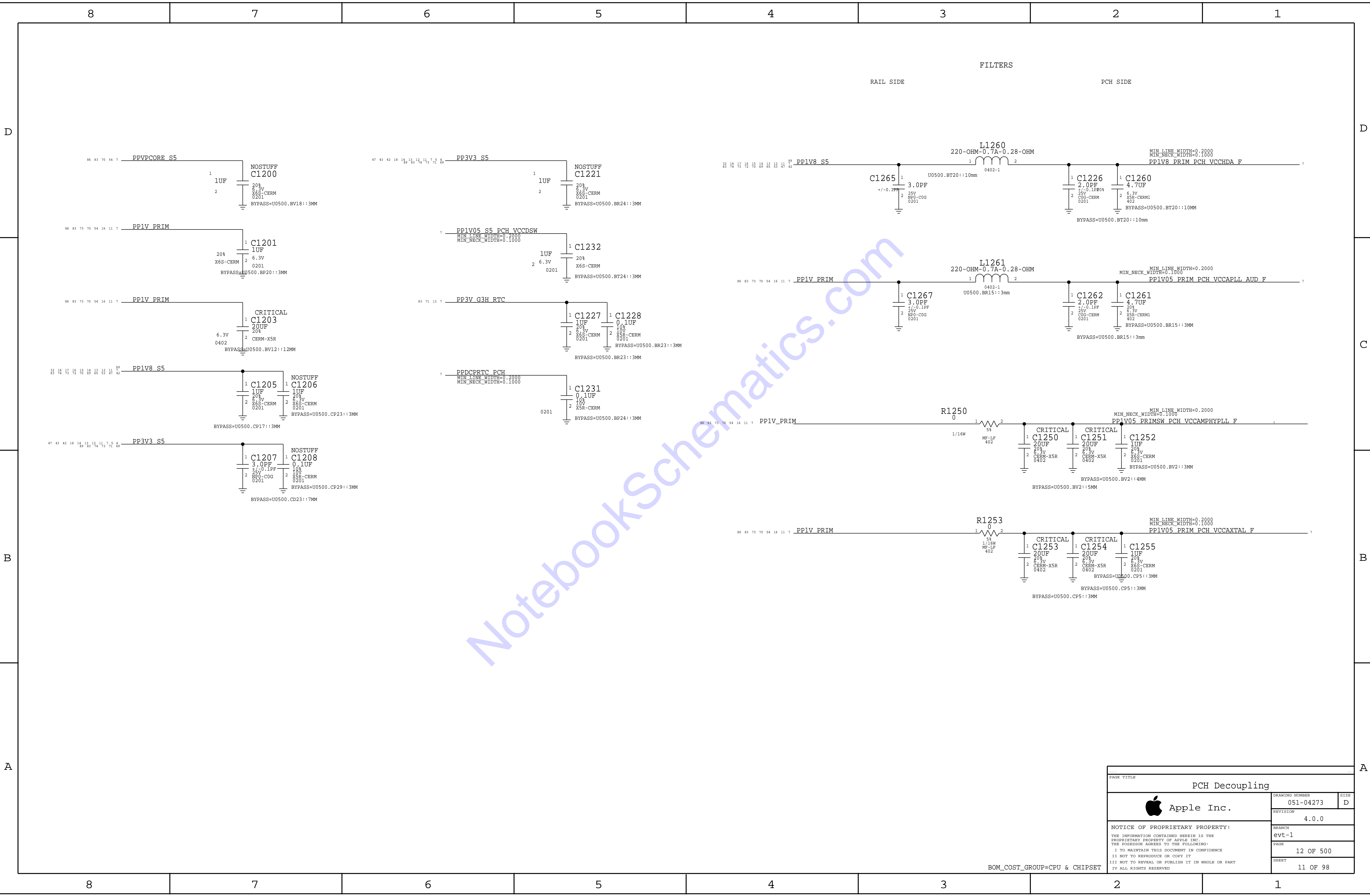



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CPU Core Decoupling		
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	PAGE	10 OF 500
	SHEET	9 OF 98



PAGE TITLE		
CPU GT Decoupling		
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	PAGE	11 OF 500
	SHEET	10 OF 98

BOM_COST_GROUP=CPU & CHIPSET



PAGE TITLE		
PCH Decoupling		
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	PAGE	12 OF 500
	SHEET	11 OF 98

D

B

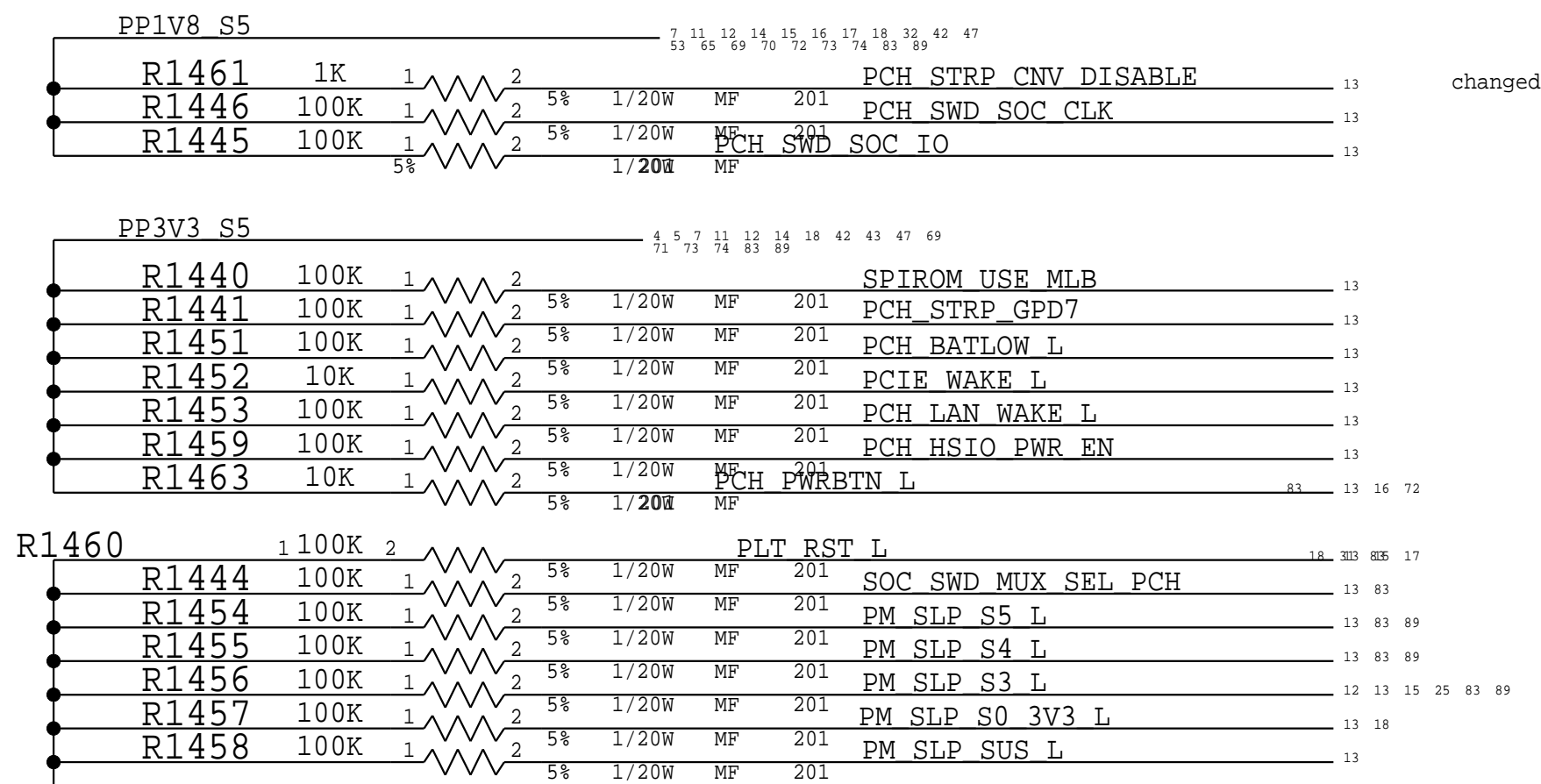
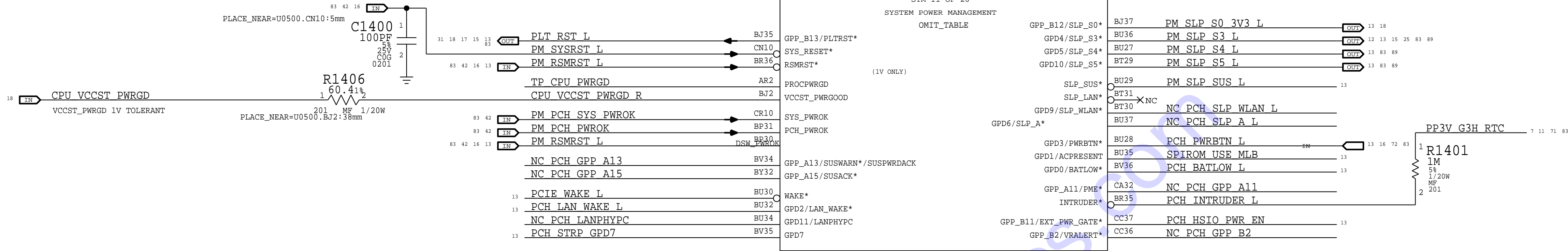
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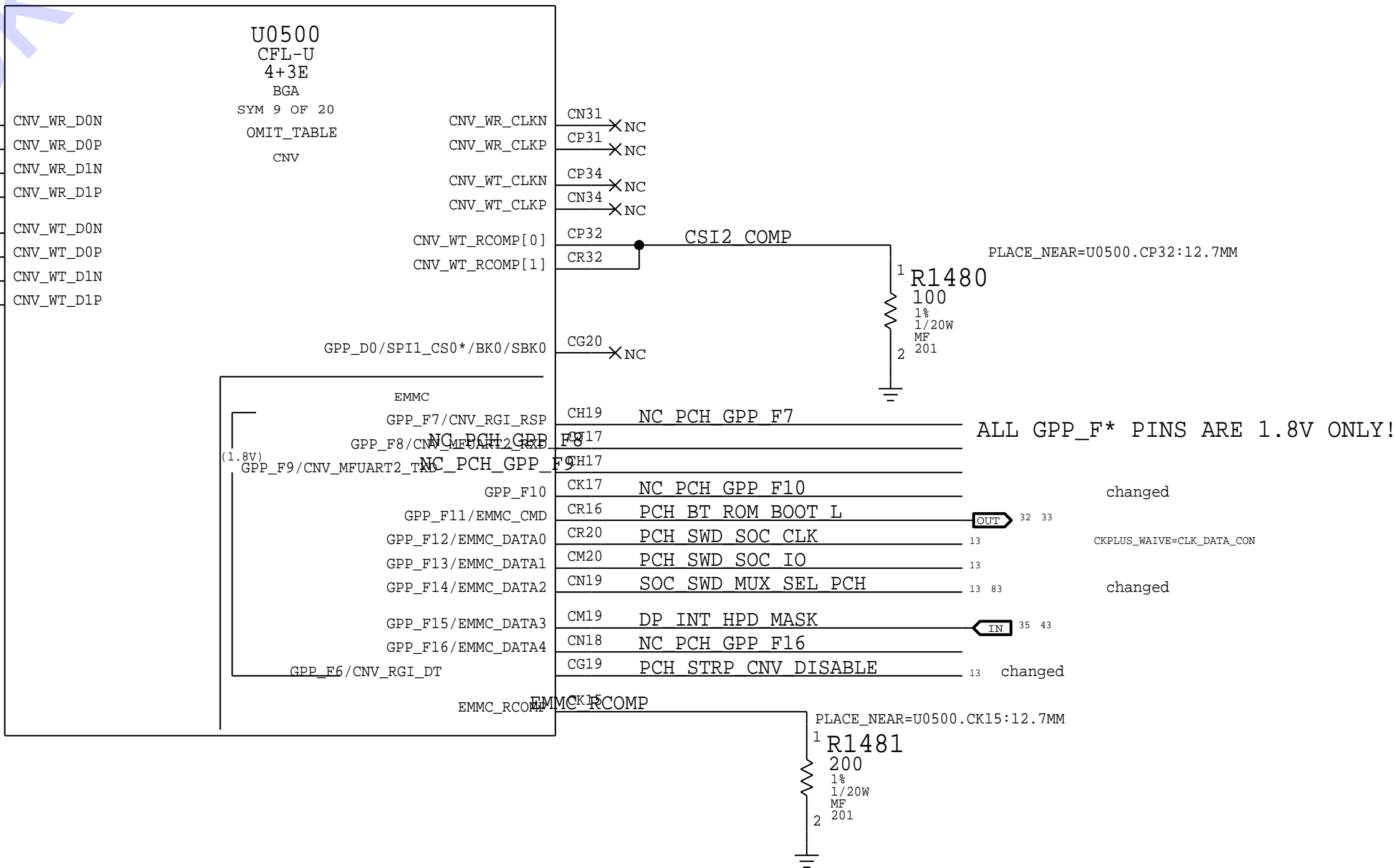
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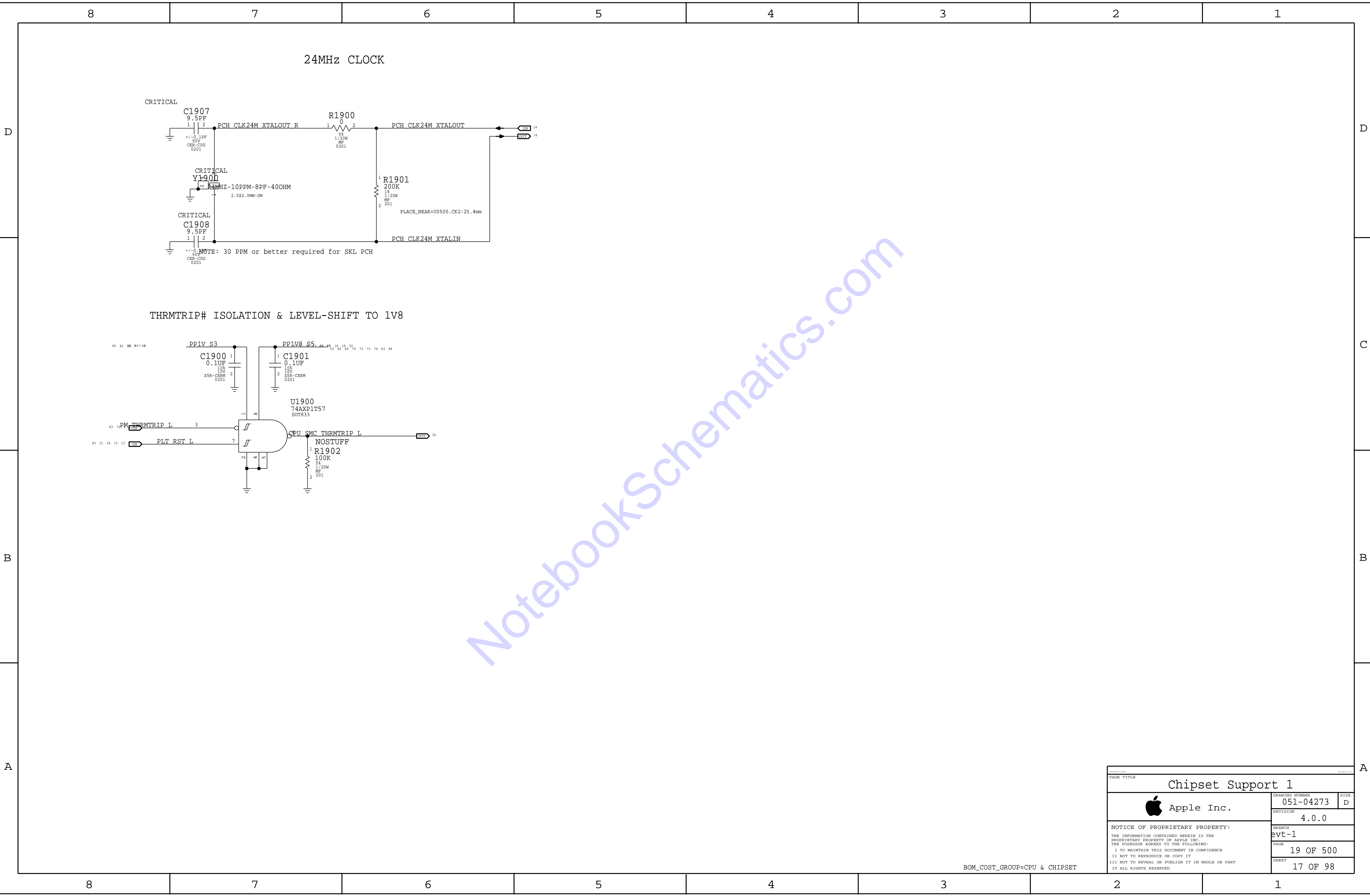


NOTE: =PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE		
PCH POWER MANAGEMENT		
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	PAGE	14 OF 500
	SHEET	13 OF 98



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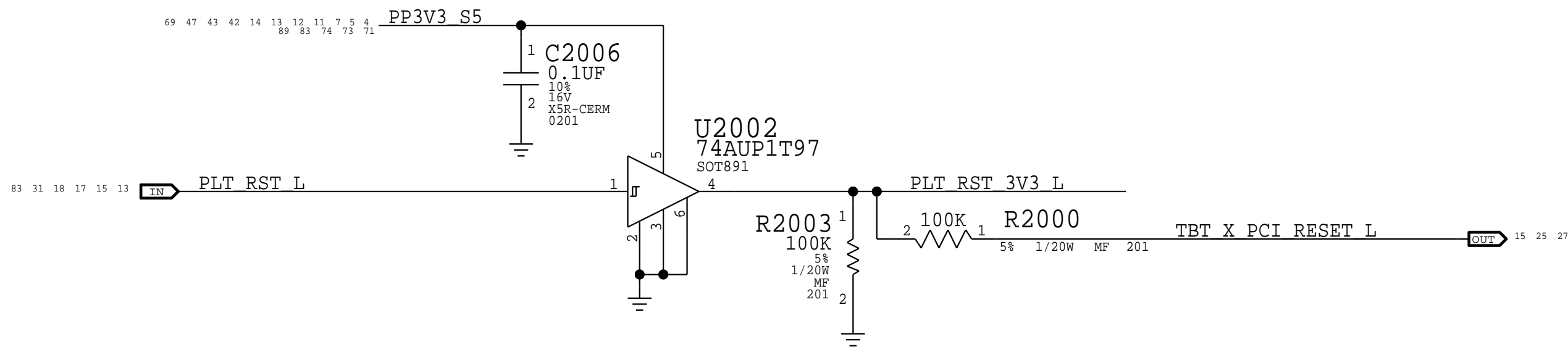
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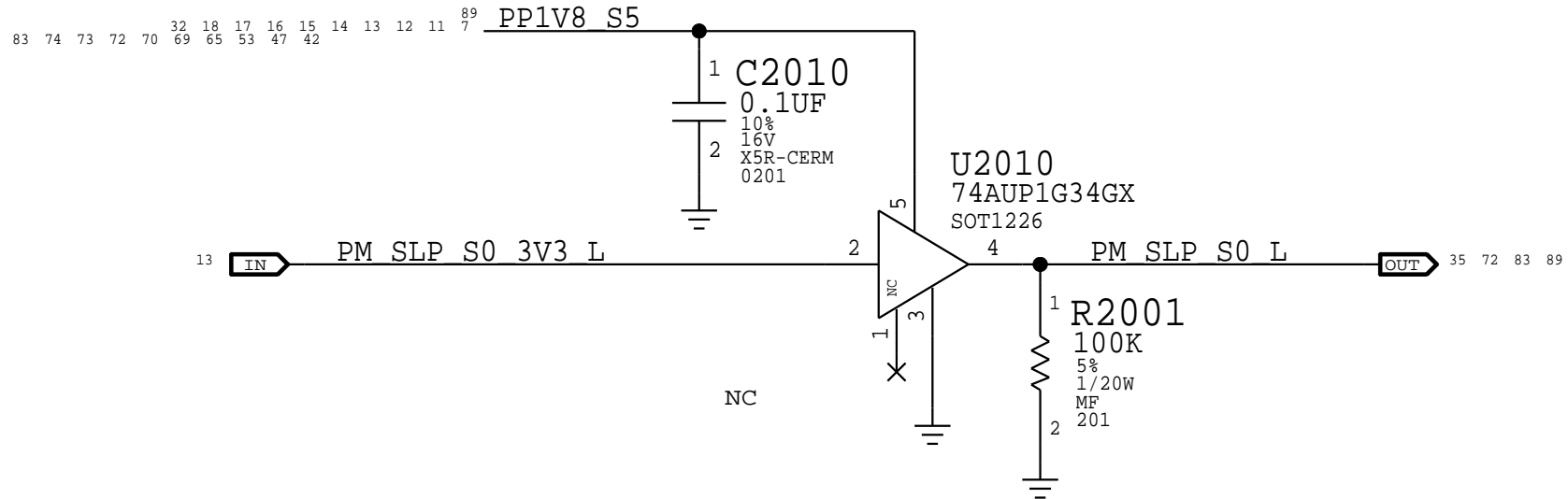
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PLATFORM RESET LEVEL-SHIFTER TO 3V3

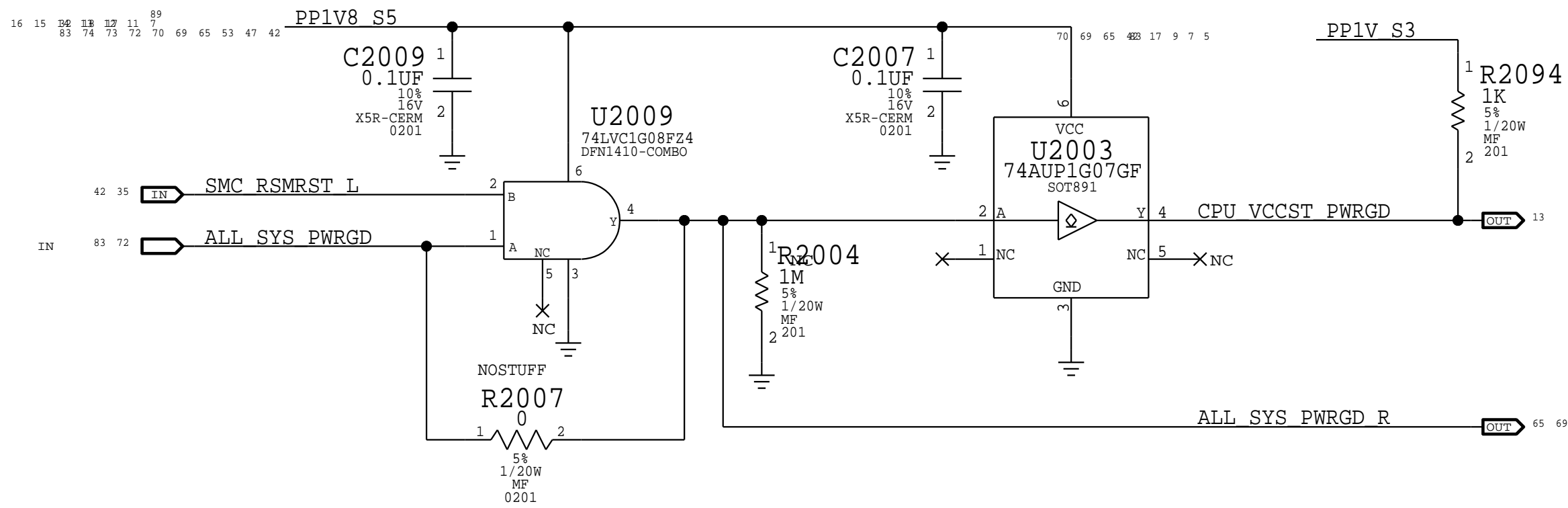


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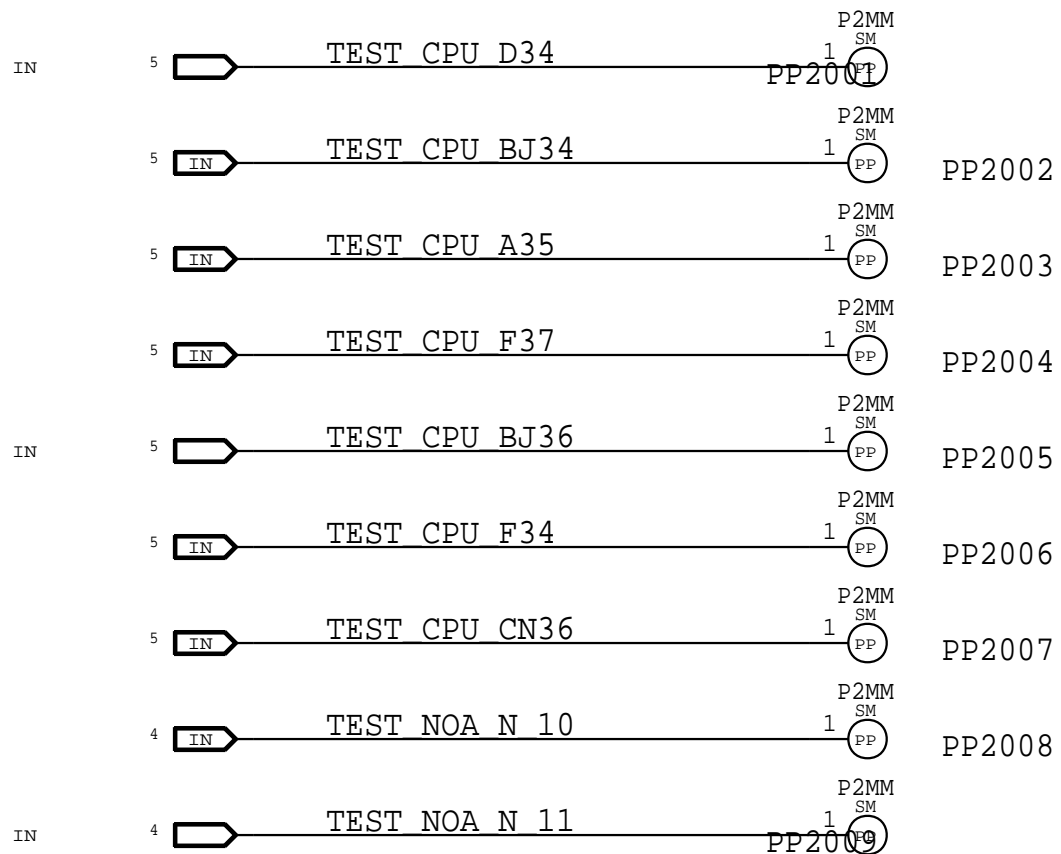


ALL_SYS_PWRGD QUALIFIER &

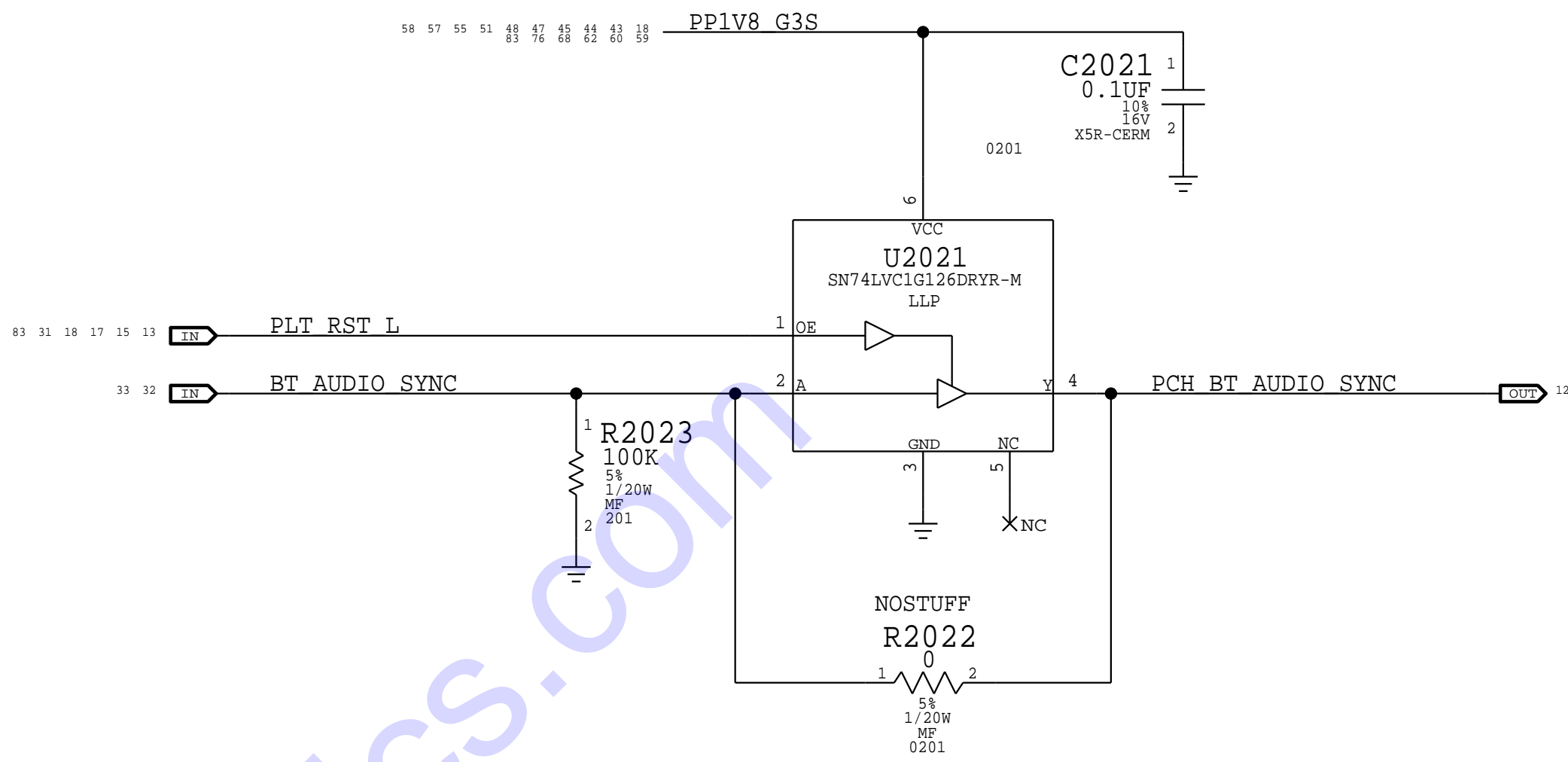
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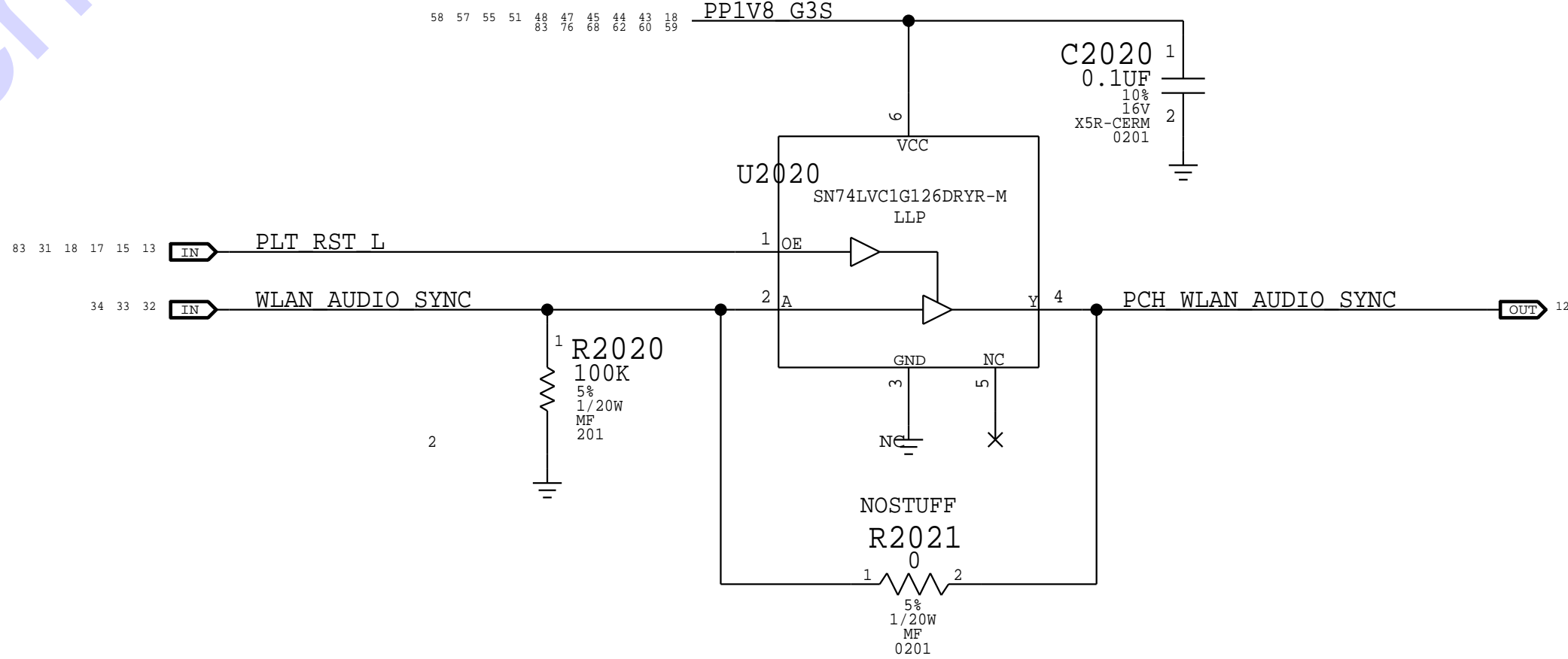
TPs for Chipset Debug Pins




BT AUDIO SYNC BUFFER



WLAN AUDIO SYNC BUFFER



PAGE TITLE		
CHIPSET SUPPORT 2		
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	REVISION	4.0.0
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	SHEET	18 OF 98

D

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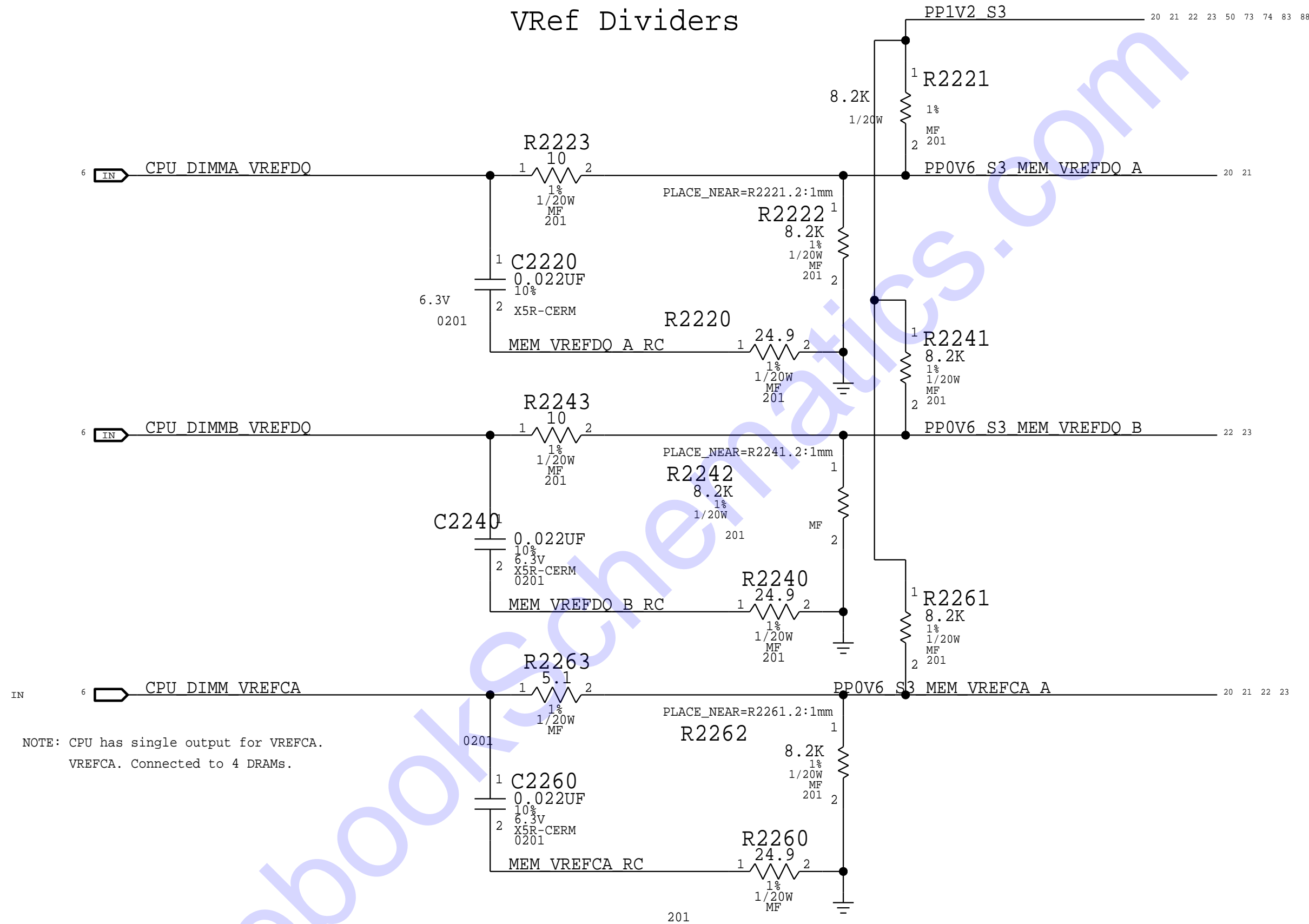
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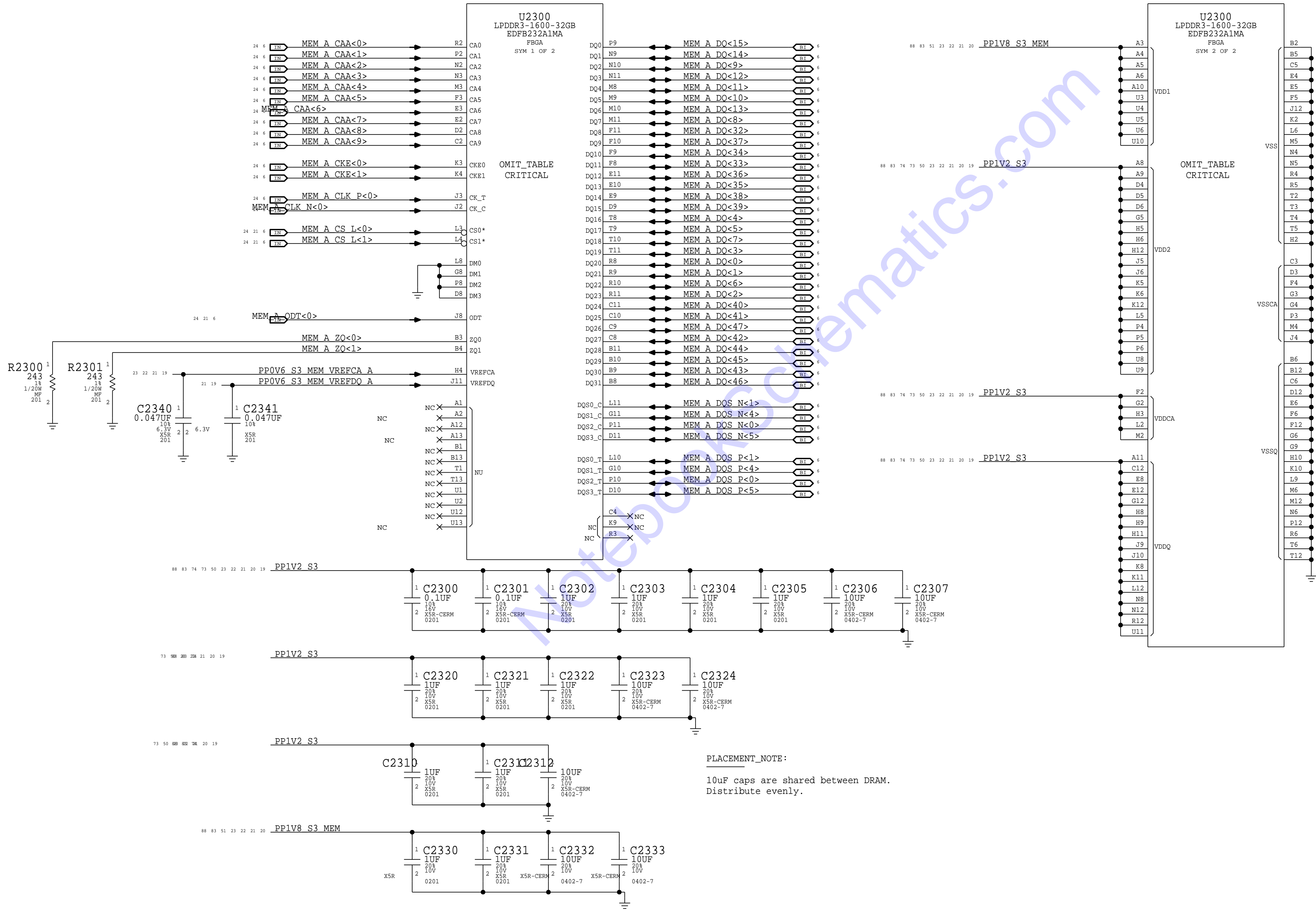
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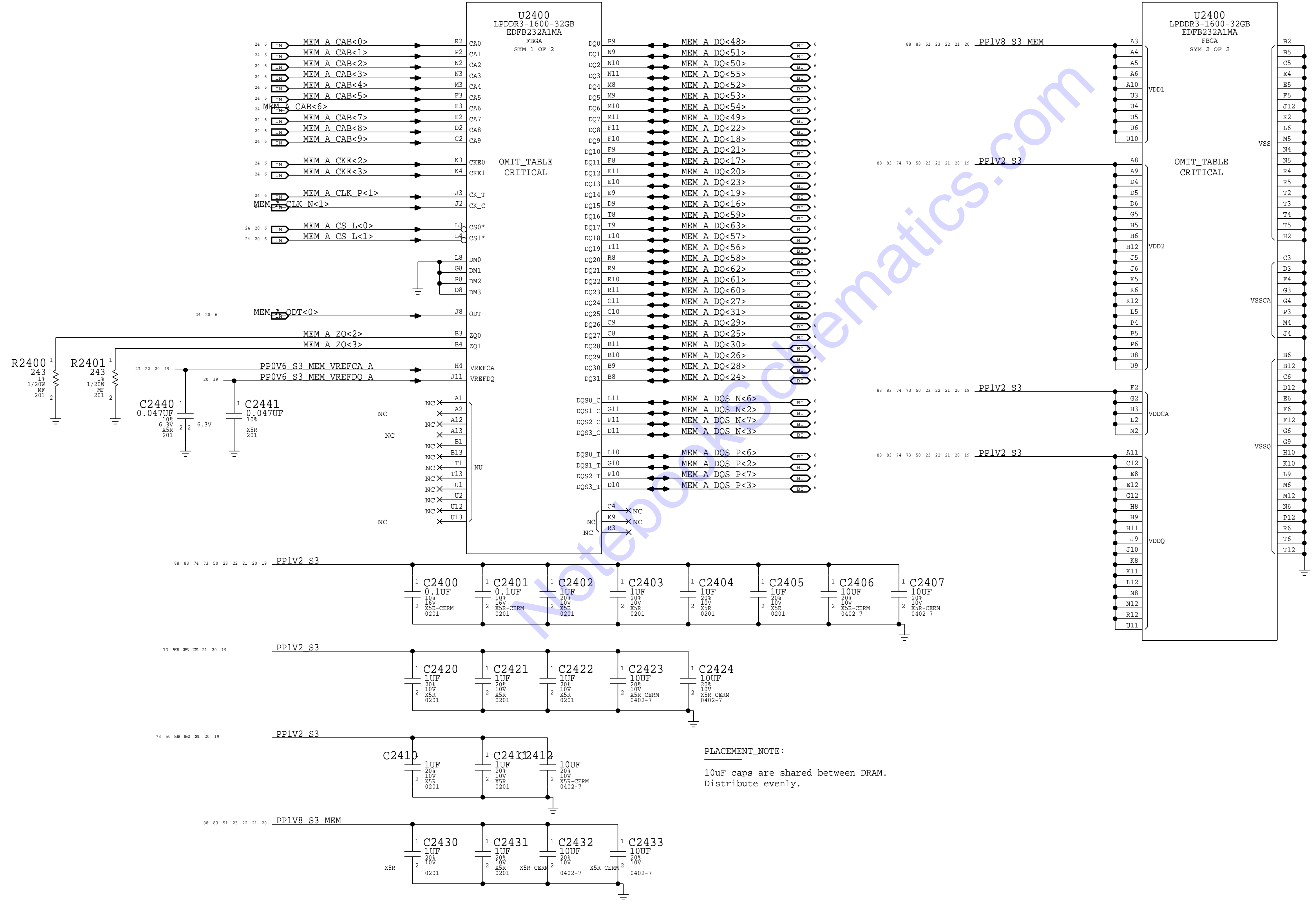
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	PAGE	22 OF 500
	SHEET	19 OF 98

LPDDR3 CHANNEL A (0-31)



PAGE TITLE		PAGE TITLE	
LPDDR3 DRAM Channel A (00-31)		LPDDR3 DRAM Channel A (00-31)	
DRAWING NUMBER		DRAWING NUMBER	
051-04273		051-04273	
REVISION		REVISION	
4.0.0		4.0.0	
BRANCH		BRANCH	
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23 OF 500		23 OF 500	
SHEET		SHEET	
20 OF 98		20 OF 98	

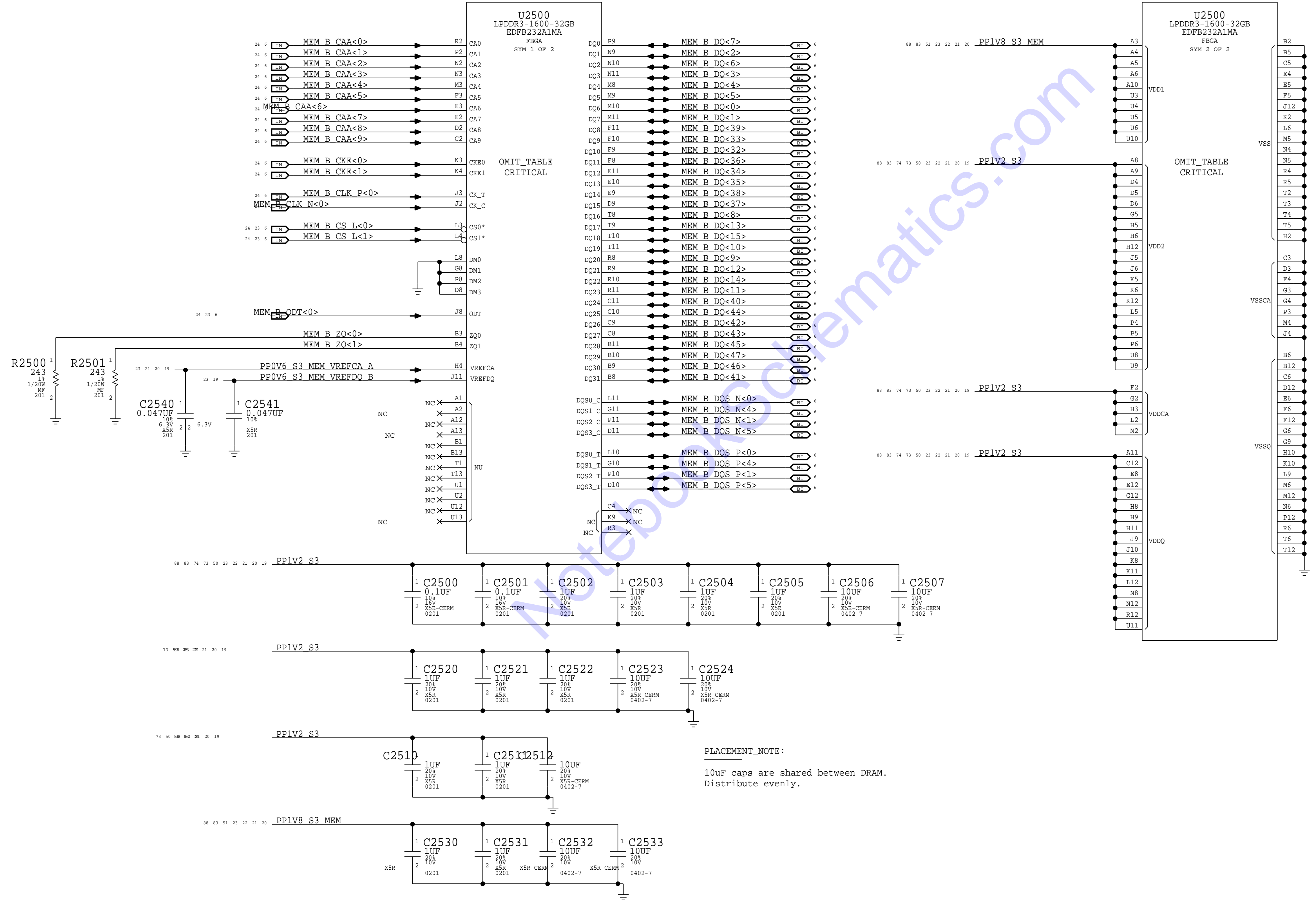
LPDDR3 CHANNEL A (32-63)



PAGE TITLE		PAGE TITLE	
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		PAGE	24 OF 500
		SHEET	21 OF 98

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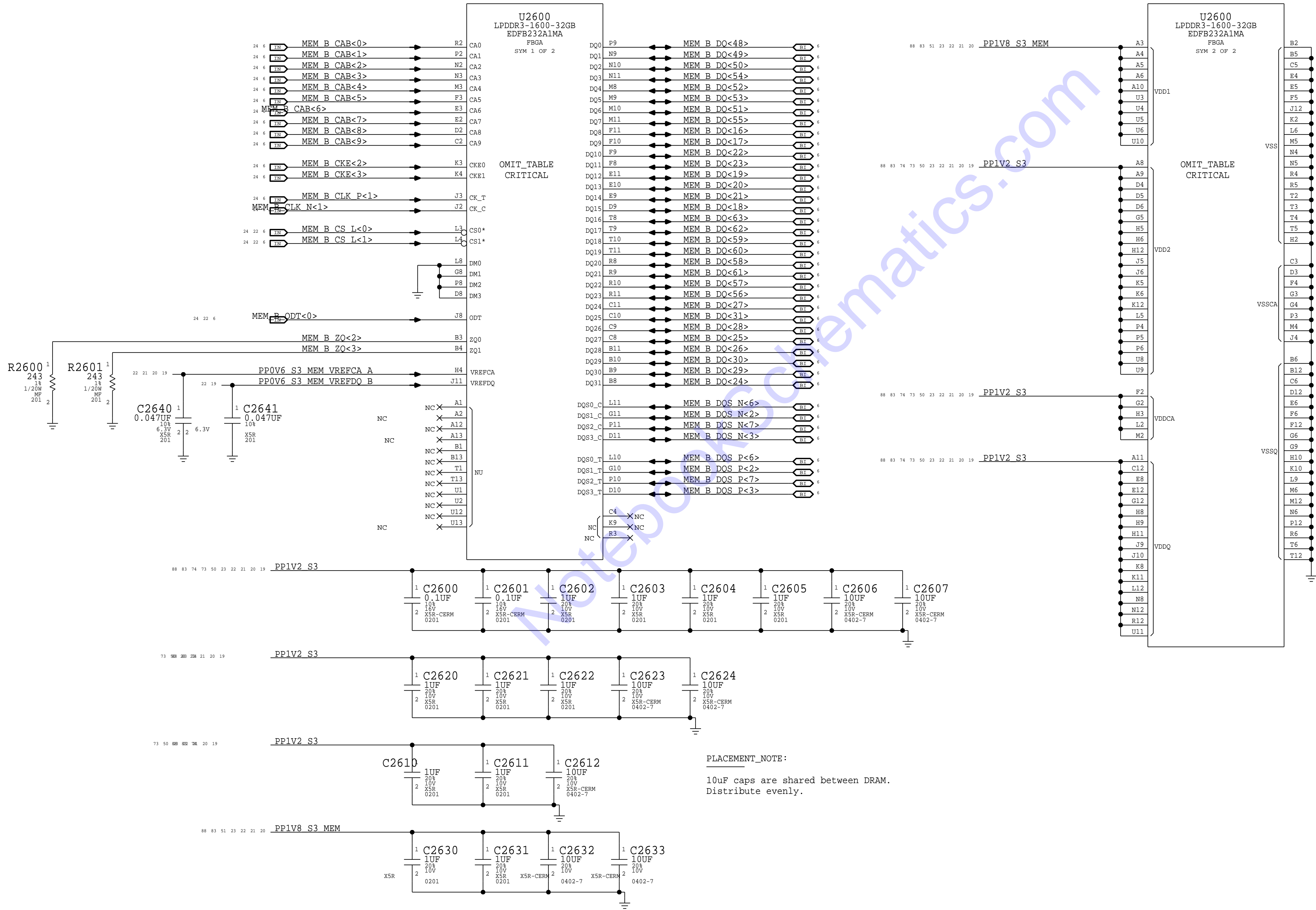
LPDDR3 CHANNEL B (0-31)



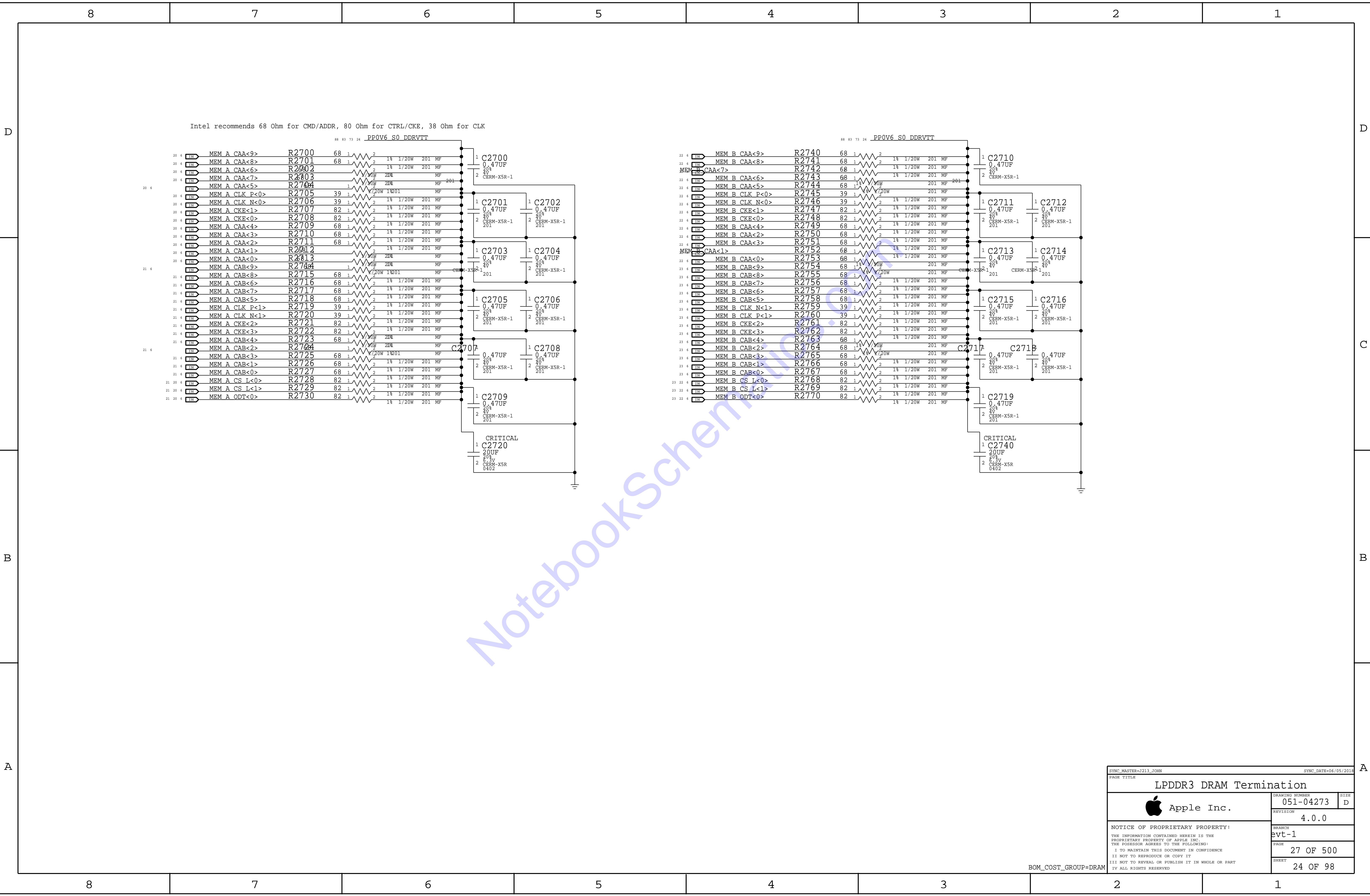
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		PAGE	25 OF 500
		SHEET	22 OF 98

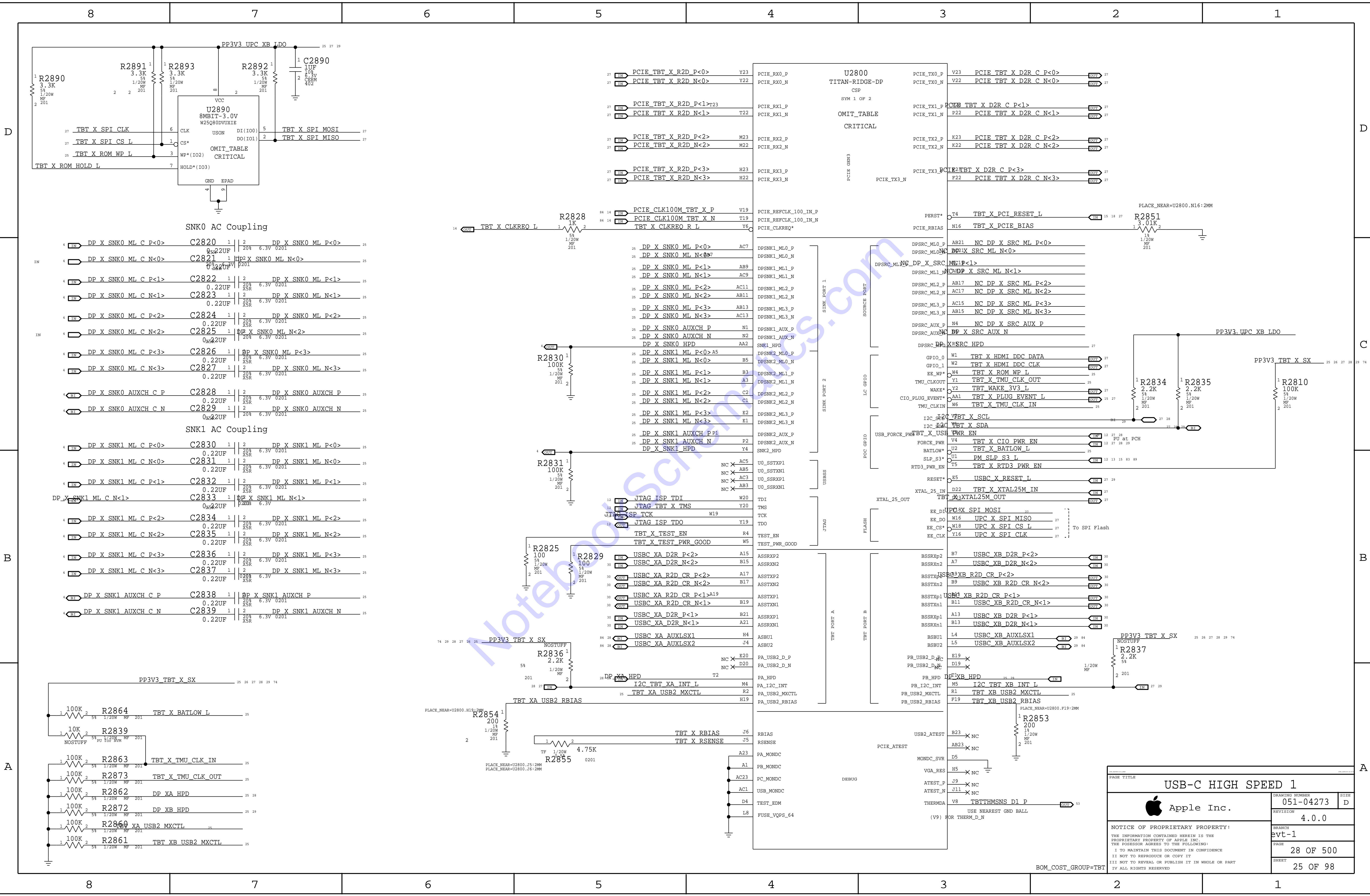
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LPDDR3 CHANNEL B (32-63)



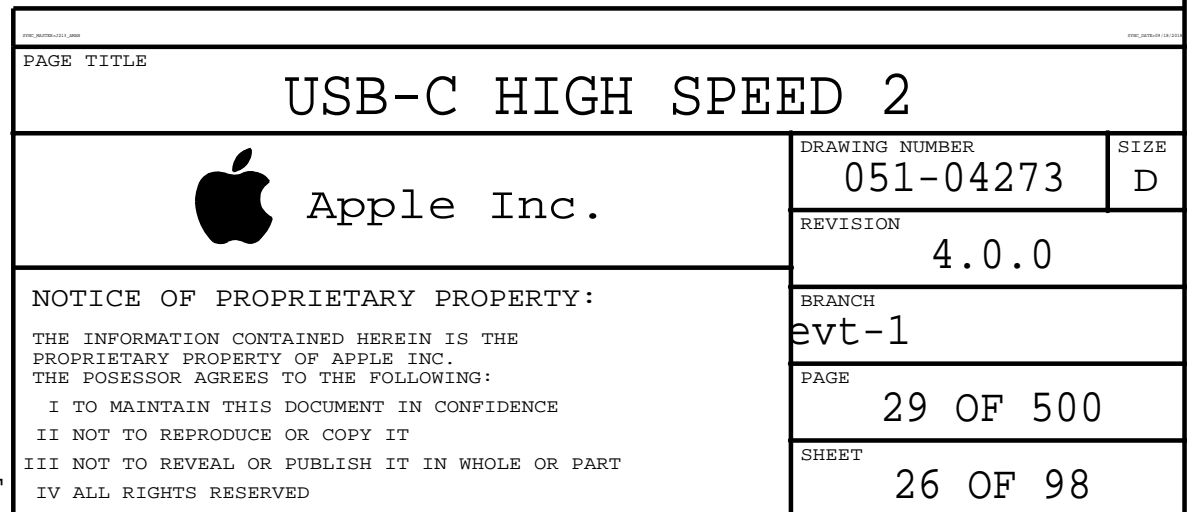
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		PAGE	26 OF 500
		SHEET	23 OF 98

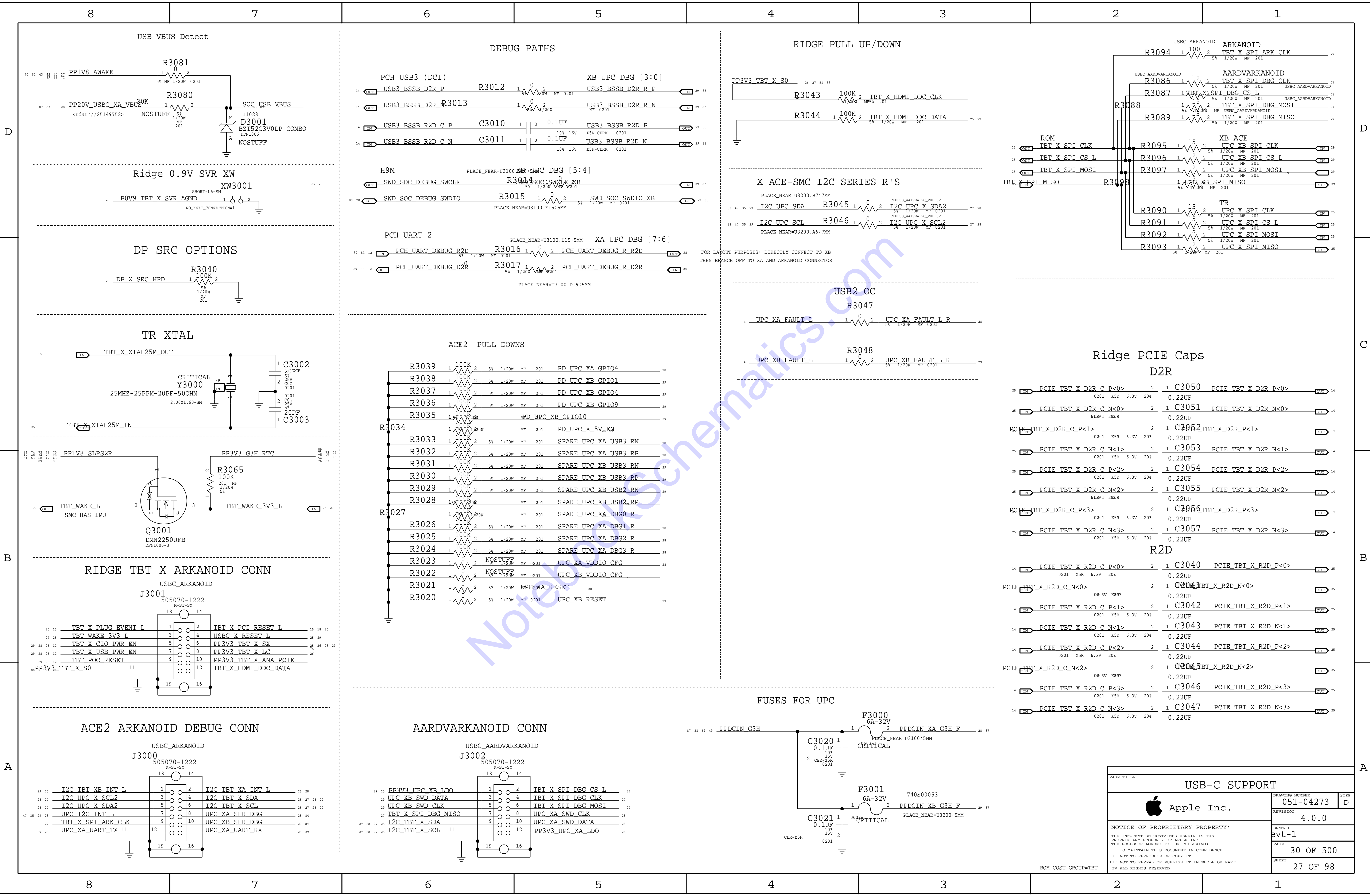




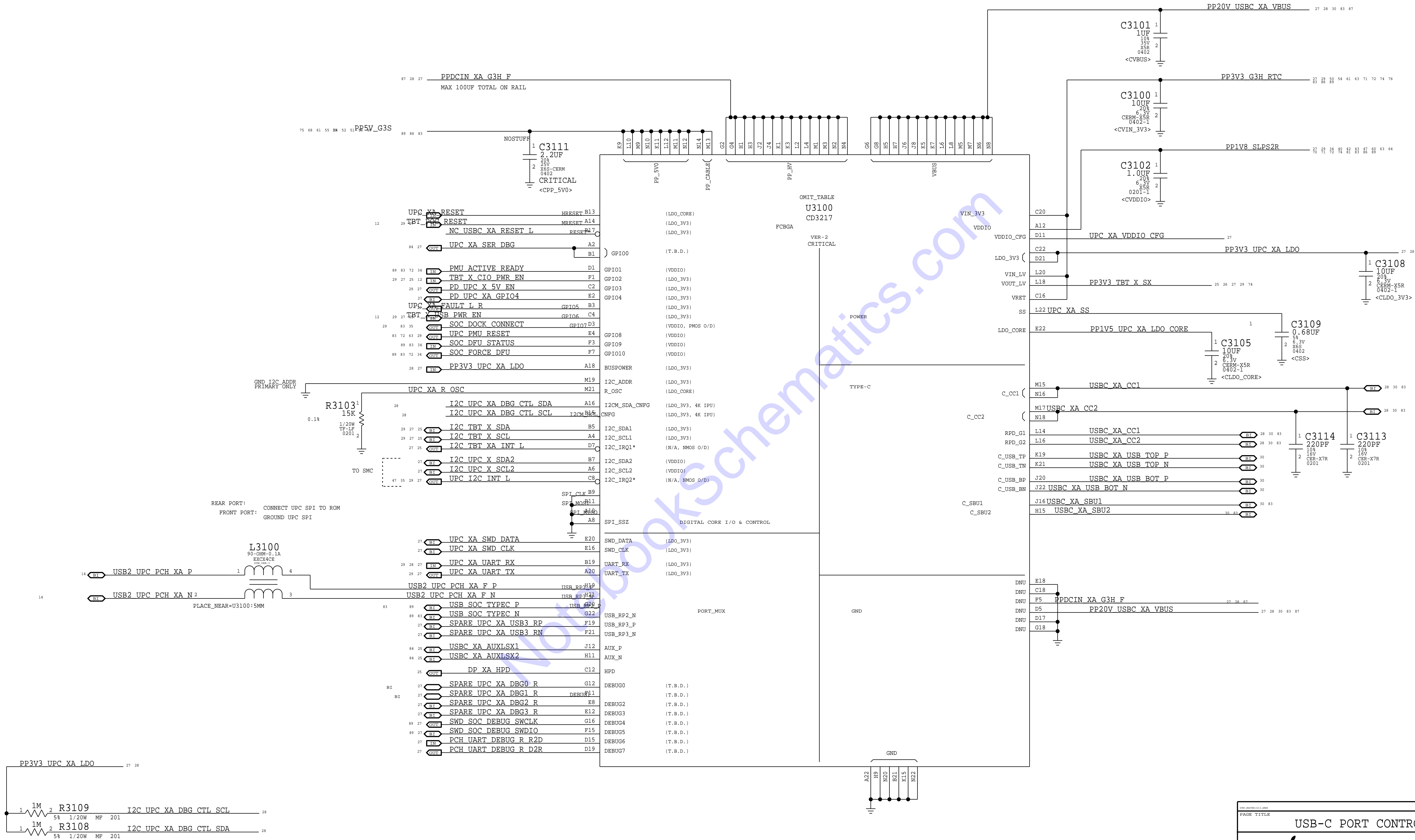
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USB-C HIGH SPEED 1		
 Apple Inc.	DRAWING NUMBER	051-04273
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	PAGE	28 OF 500
	SHEET	25 OF 98

BOM_COST_GROUP=TBT





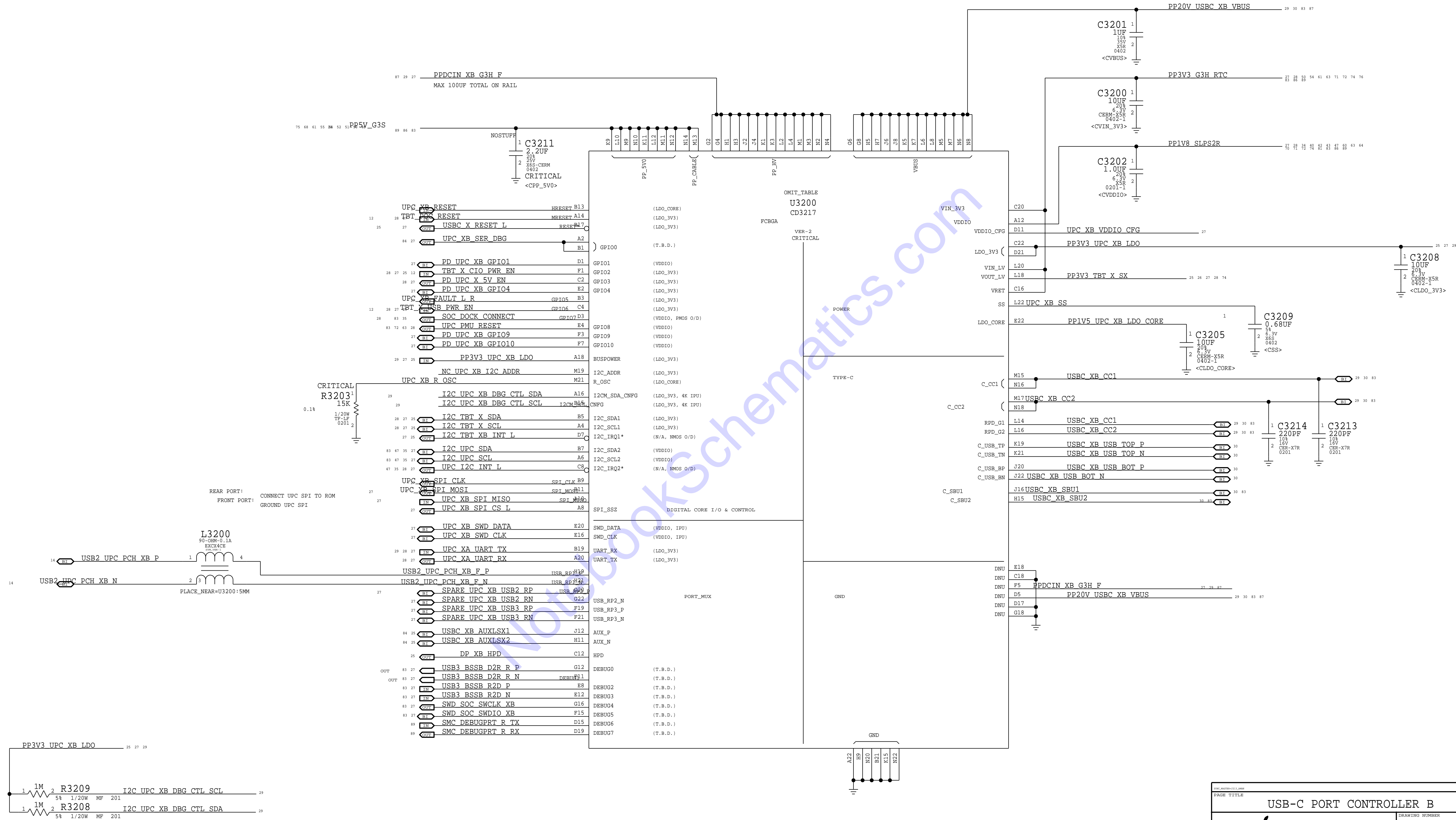
PRIMARY USB-C PORT CONTROLLER (UPC) [FRONT LEFT]



PAGE TITLE		
USB-C PORT CONTROLLER A		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
	BRANCH	evt-1
	PAGE	31 OF 500
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BOM_COST_GROUP=USB-C

SECONDARY USB-C PORT CONTROLLER (UPC) [REAR LEFT]



D

B

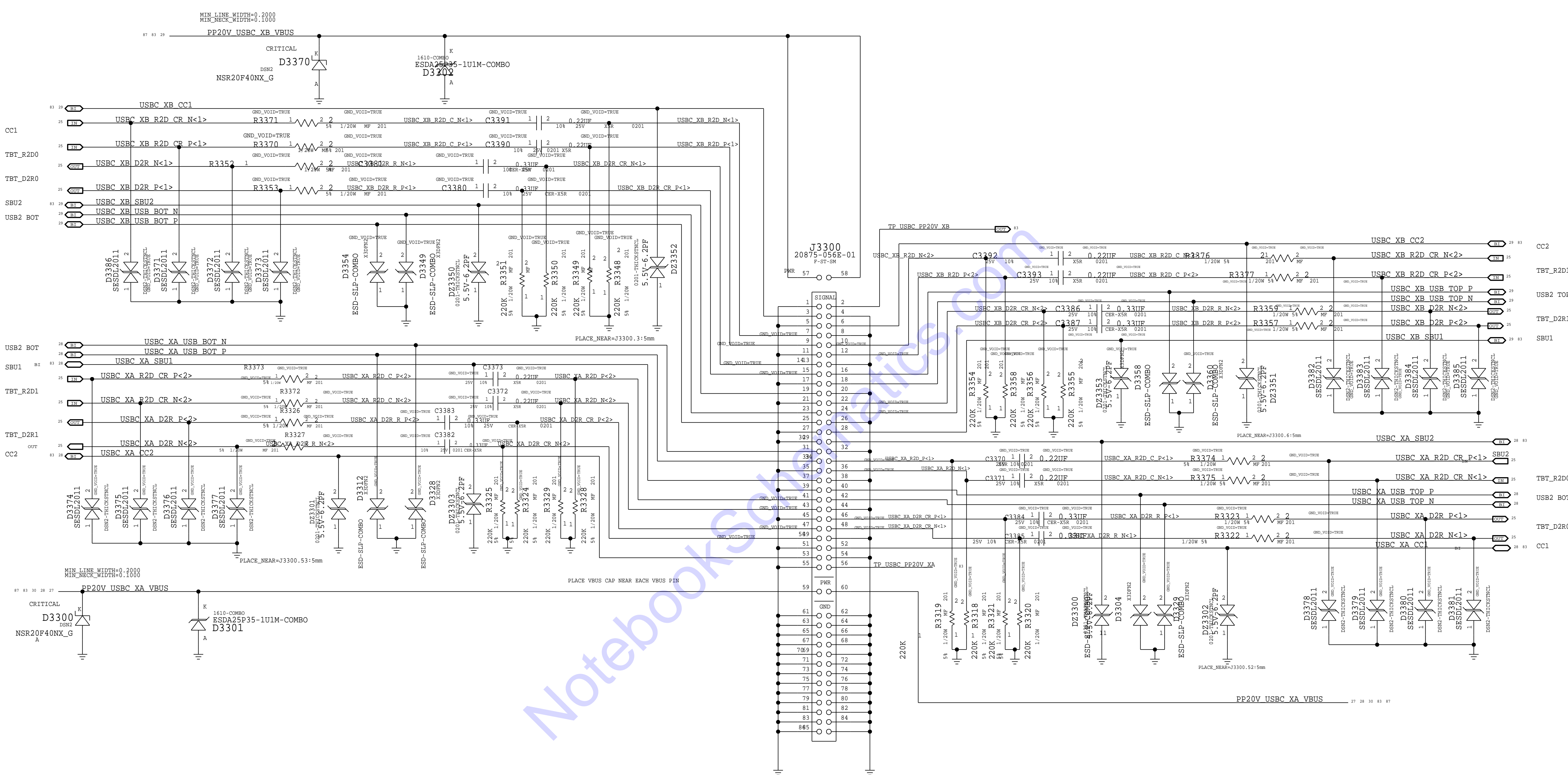
A


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LAST CHANGE: Wed Apr 1 22:57:37 2015			
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USB-C CONNECTOR A			
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	PAGE	33 OF 500	
	SHEET	30 OF 98	

BOM_COST_GROUP=USB-C

D

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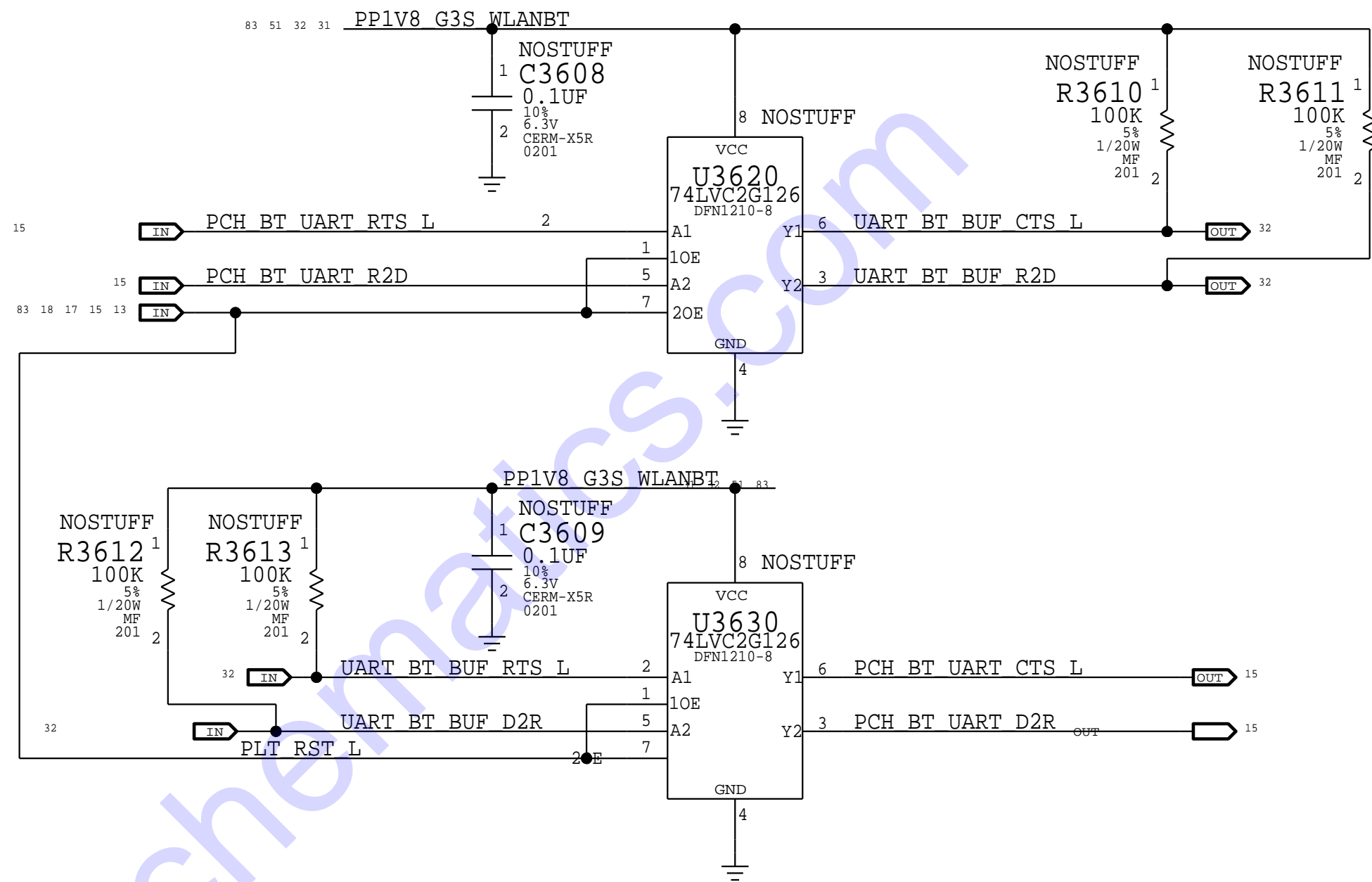
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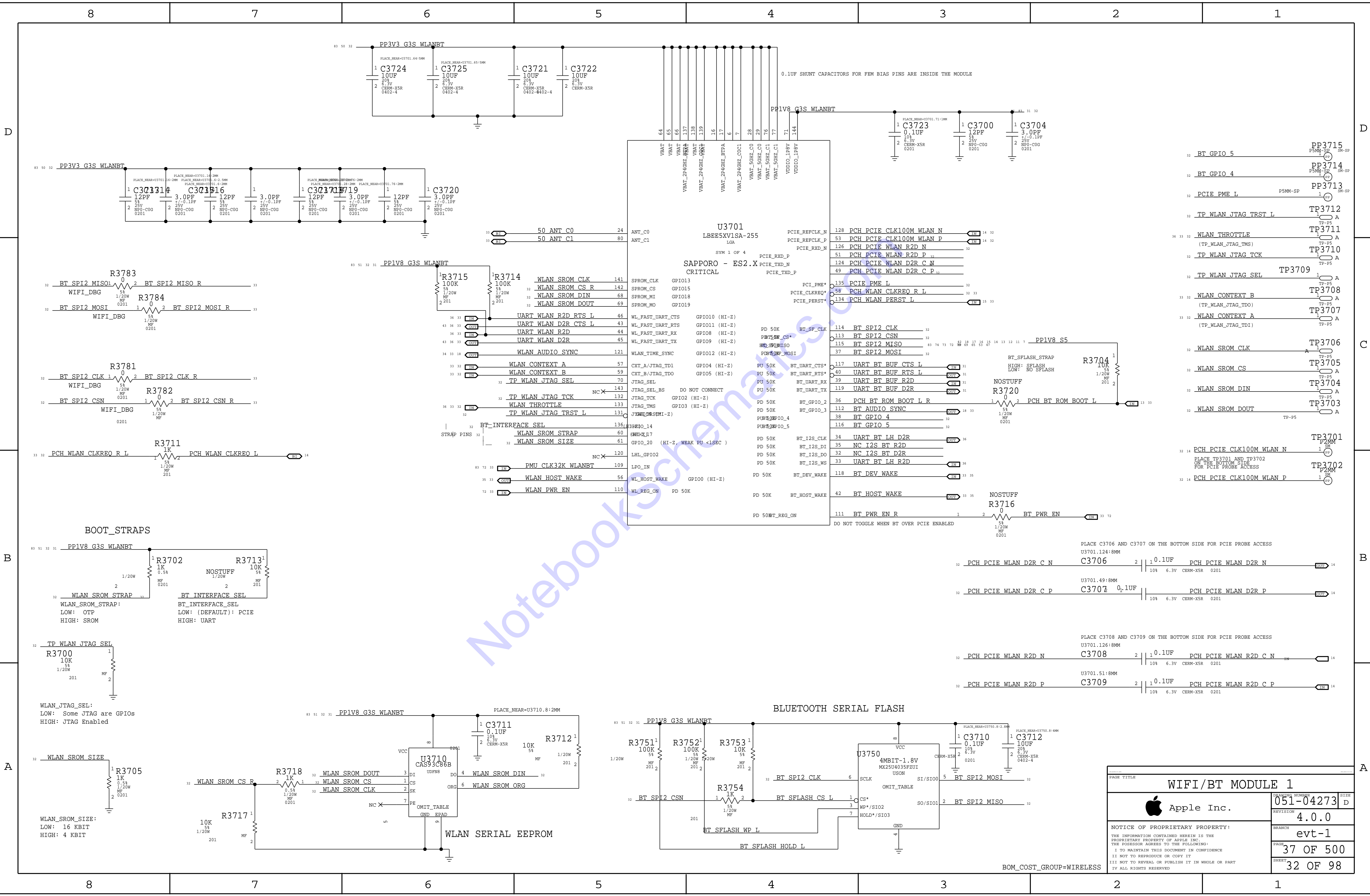
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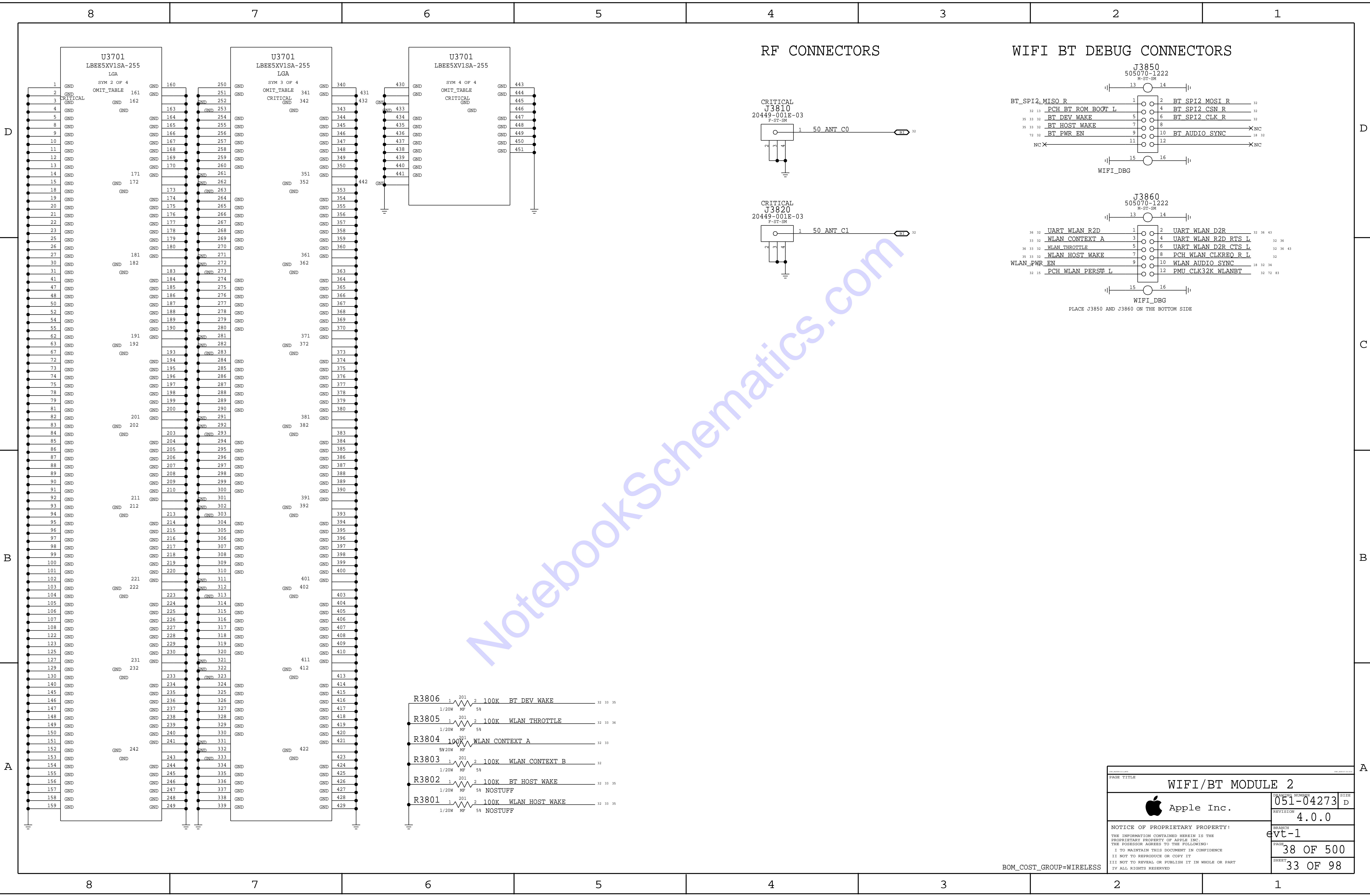


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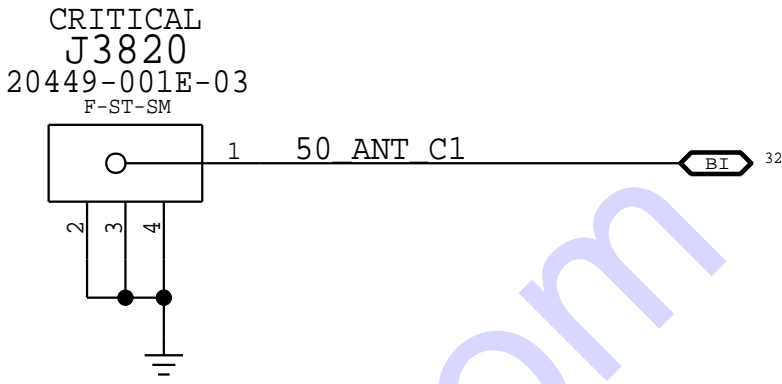
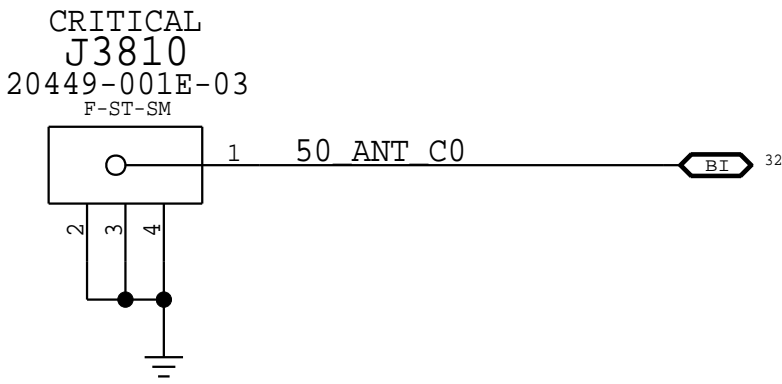
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WIFI/BT SUPPORT		
 Apple Inc.	DRAWING NUMBER	051-04273
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	PAGE	36 OF 500
	SHEET	31 OF 98



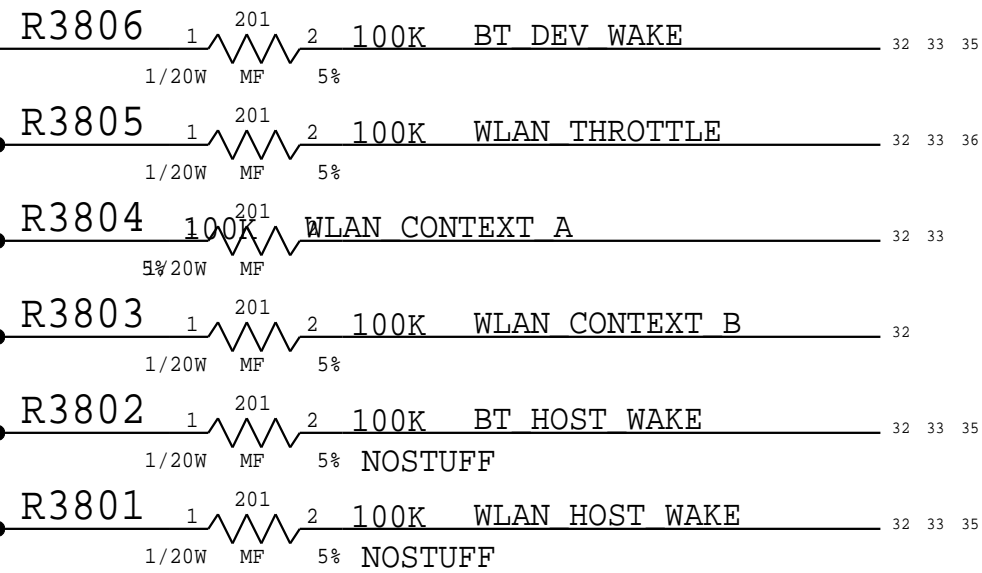
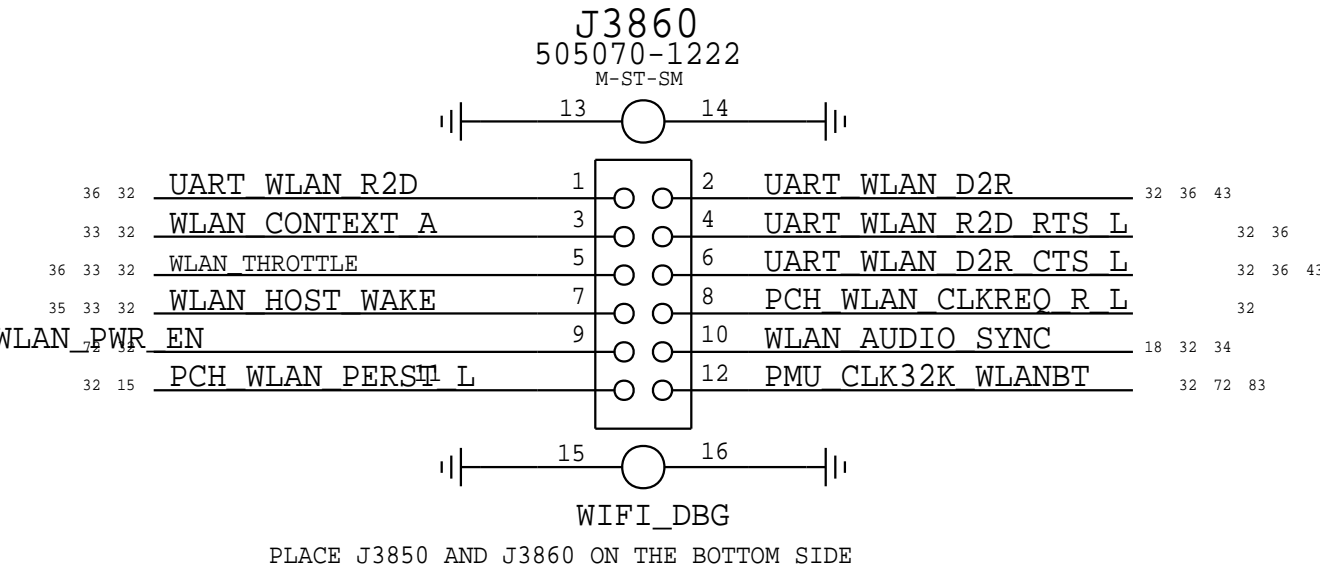
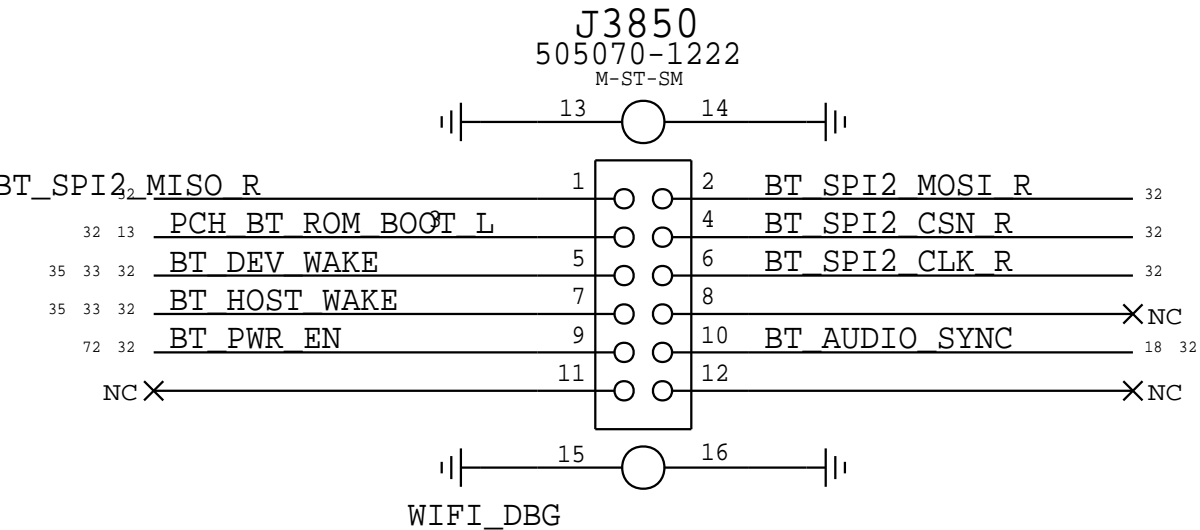
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	PAGE	37 OF 500	
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SHEET			
32 OF 98			



RF CONNECTORS

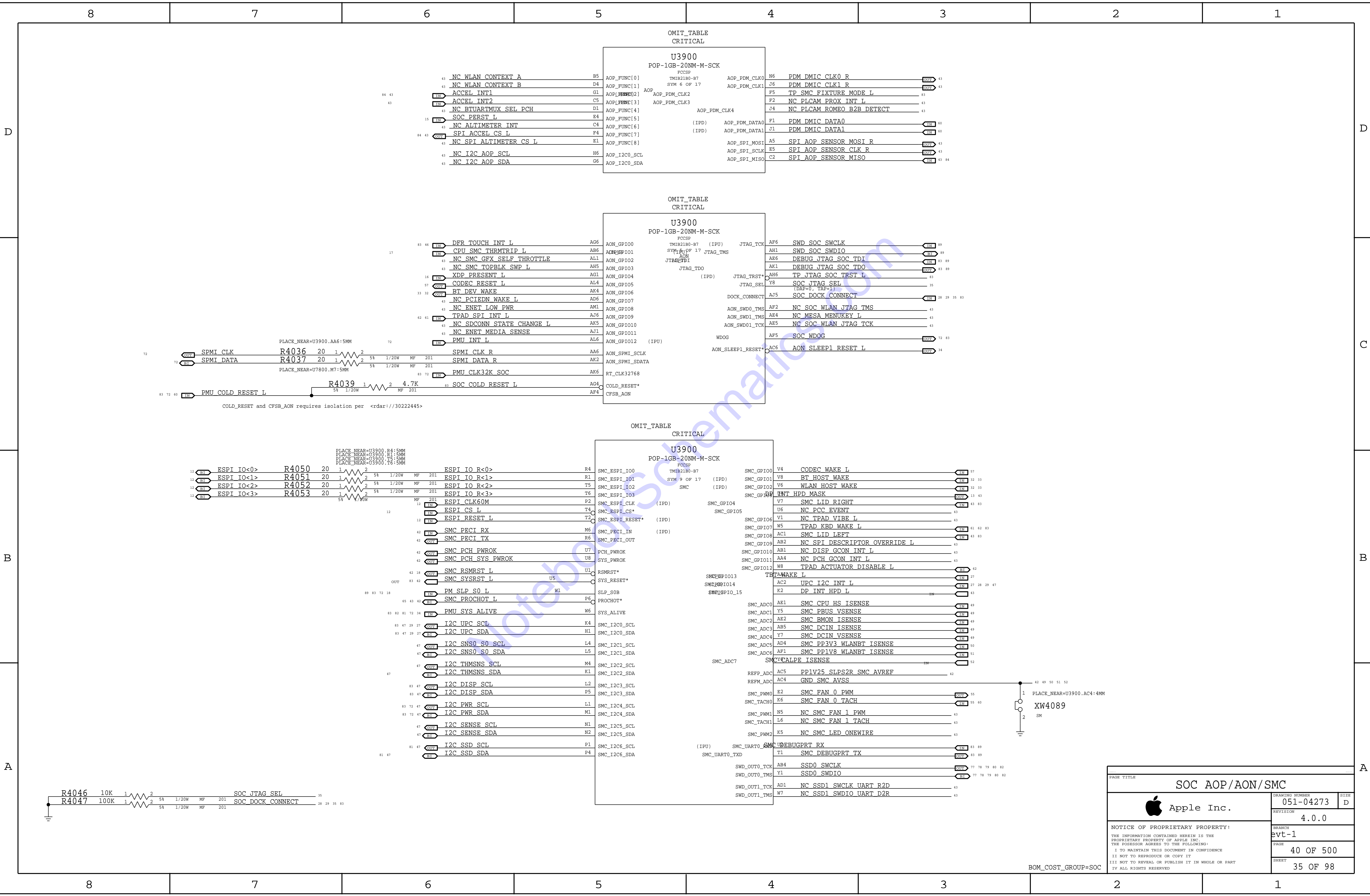


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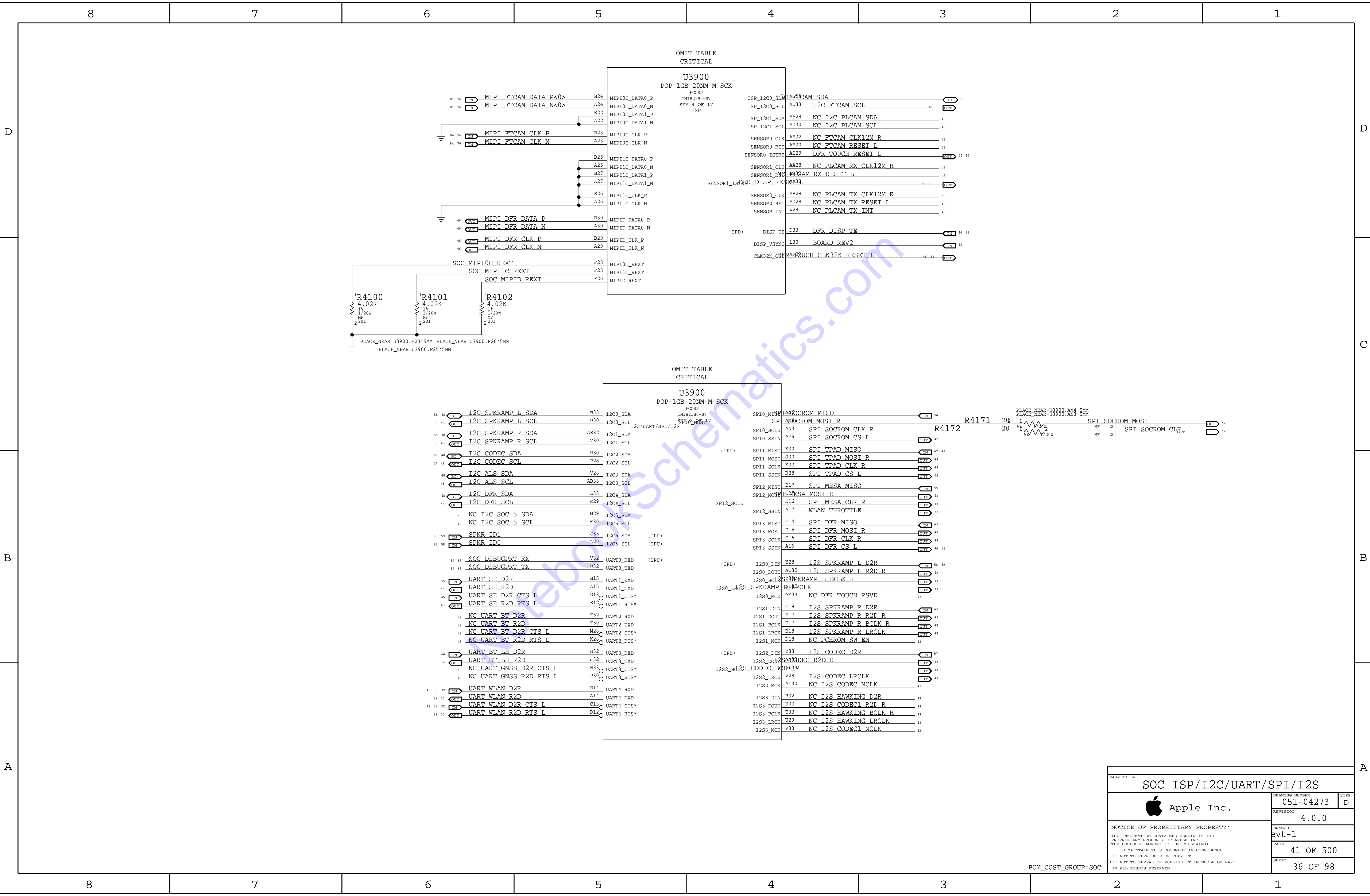


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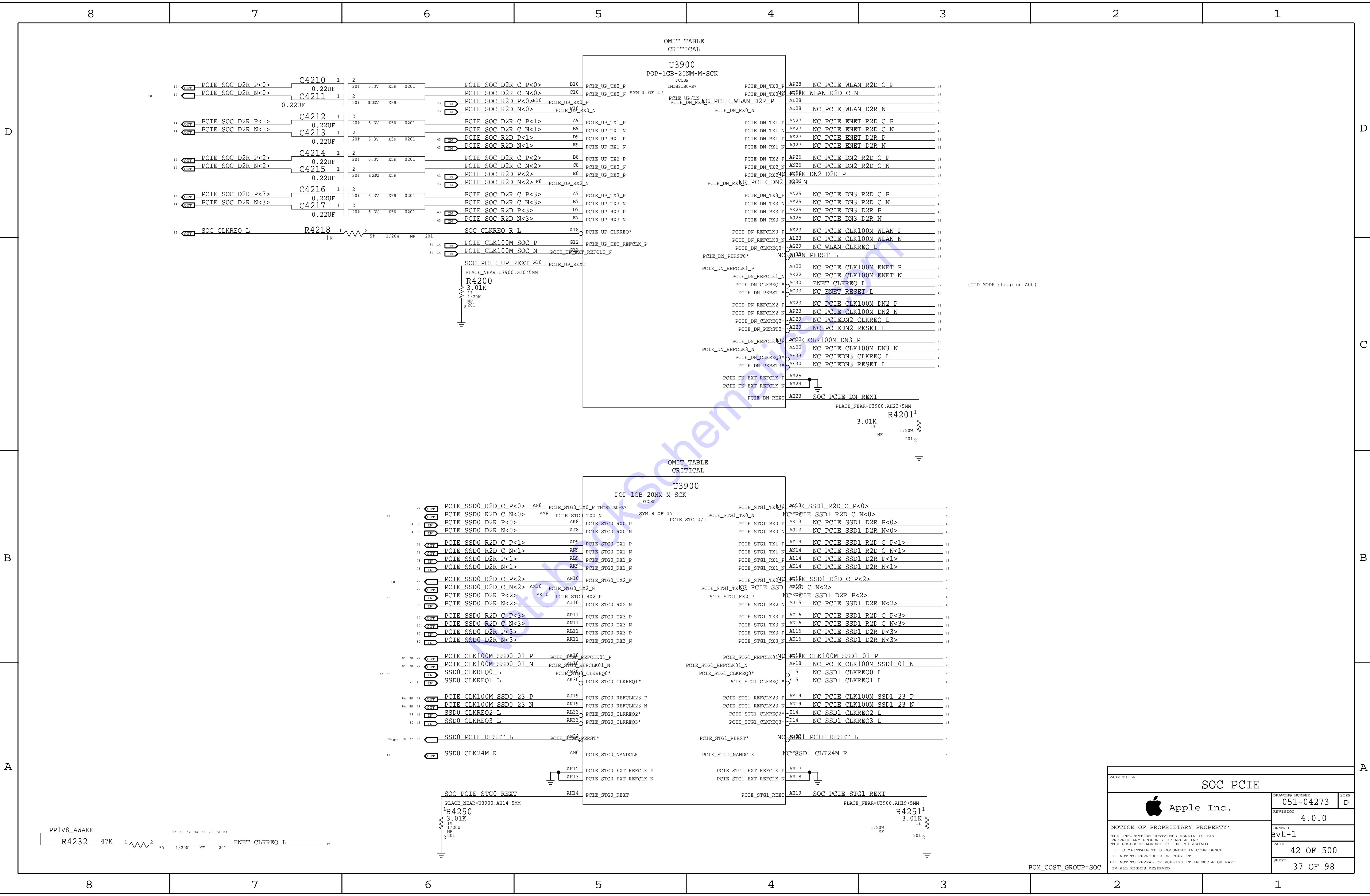
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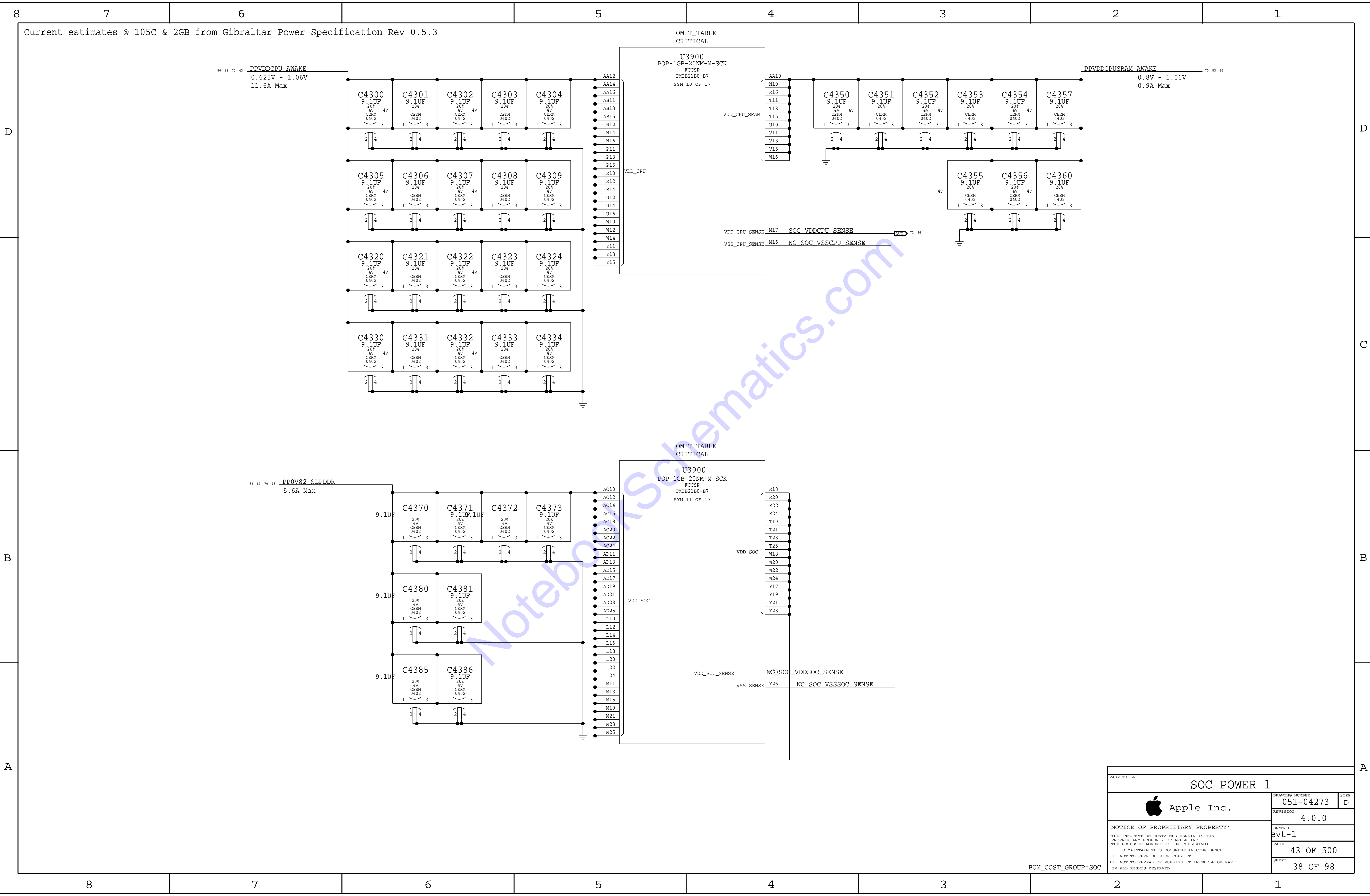


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	REVISION	4.0.0
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41 OF 500		
36 OF 98		



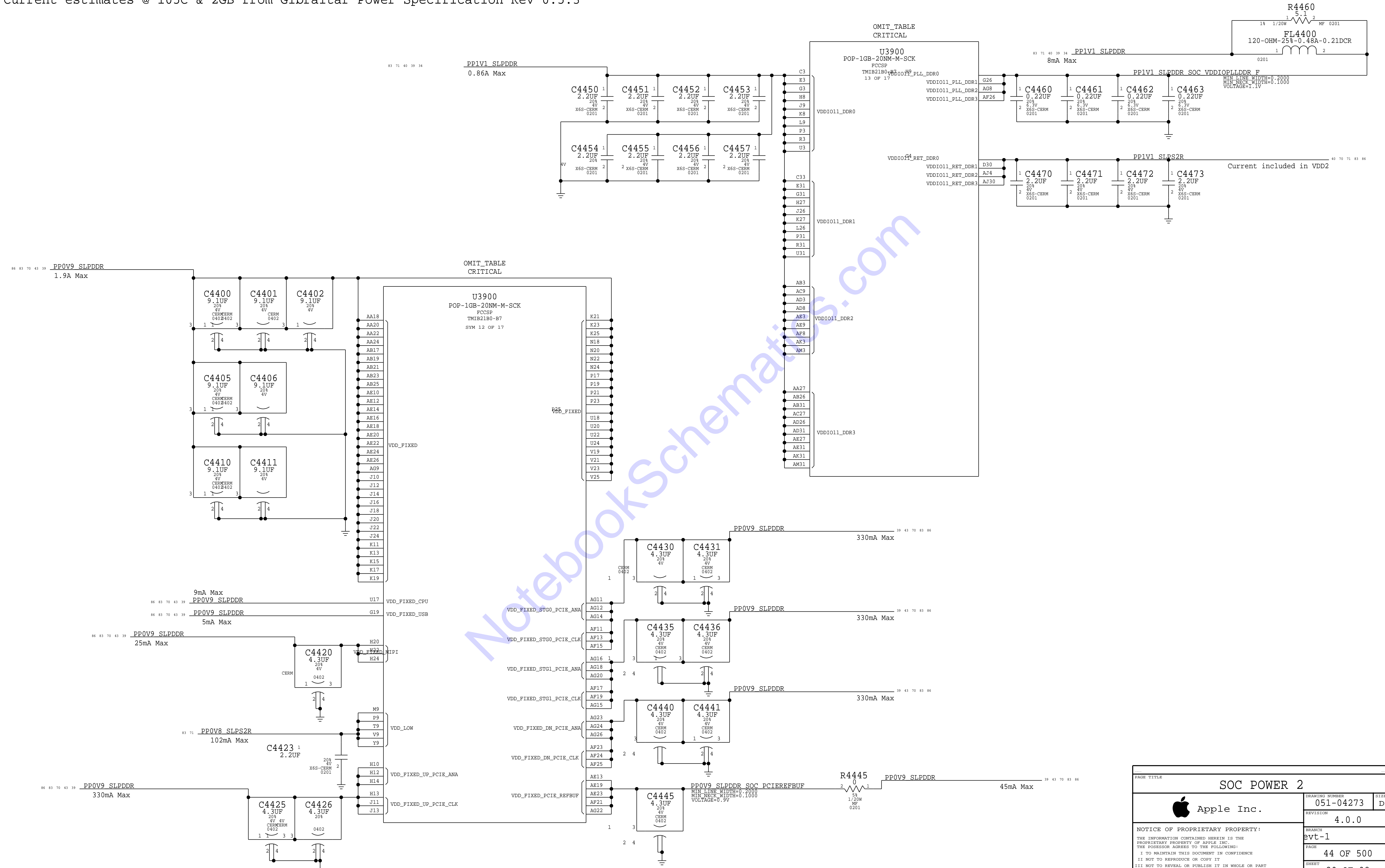
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	SHEET	37 OF 98

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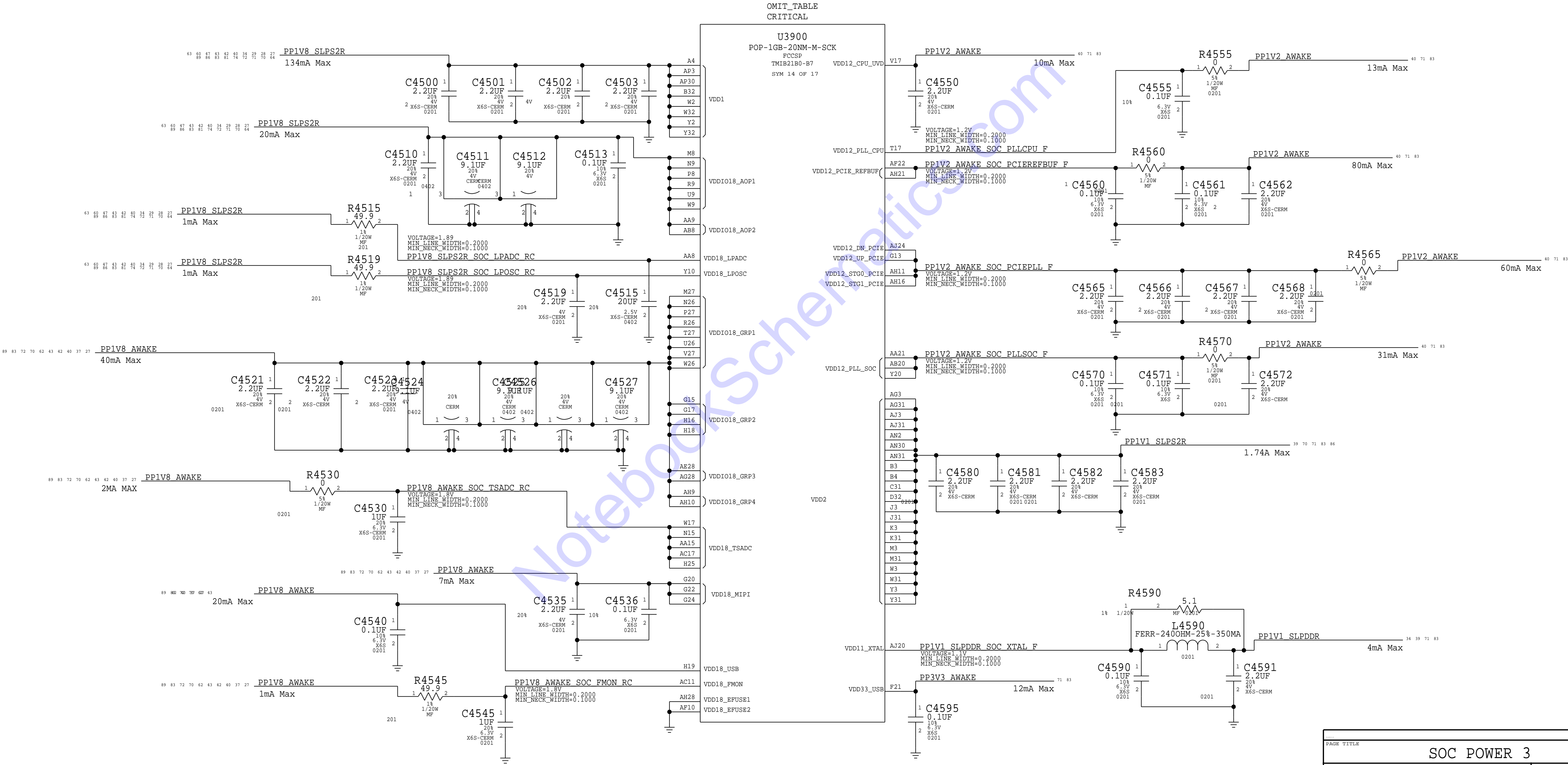
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	PAGE	43 OF 500
	SHEET	38 OF 98


Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



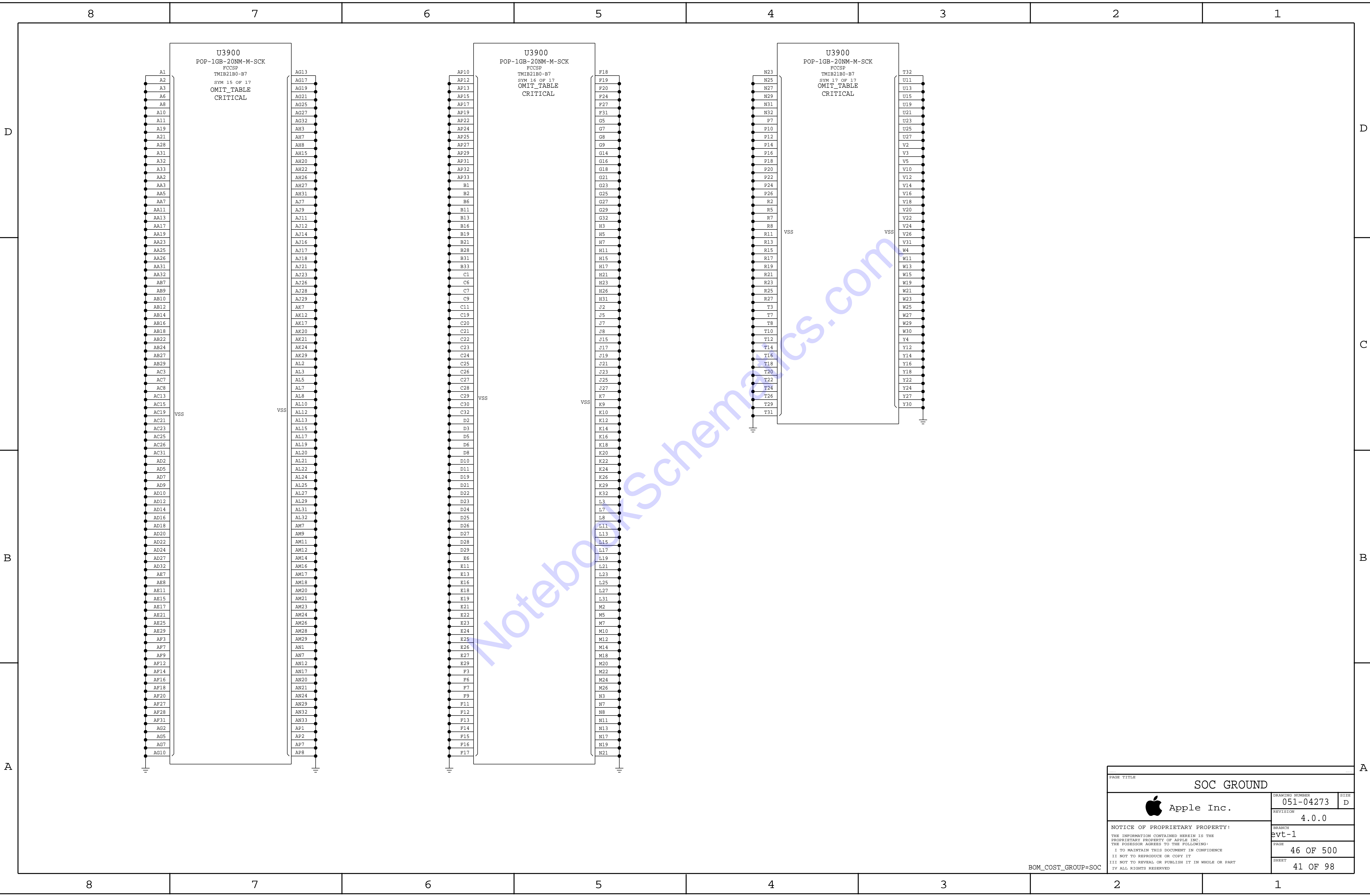
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	PAGE	44 OF 500
	SHEET	39 OF 98


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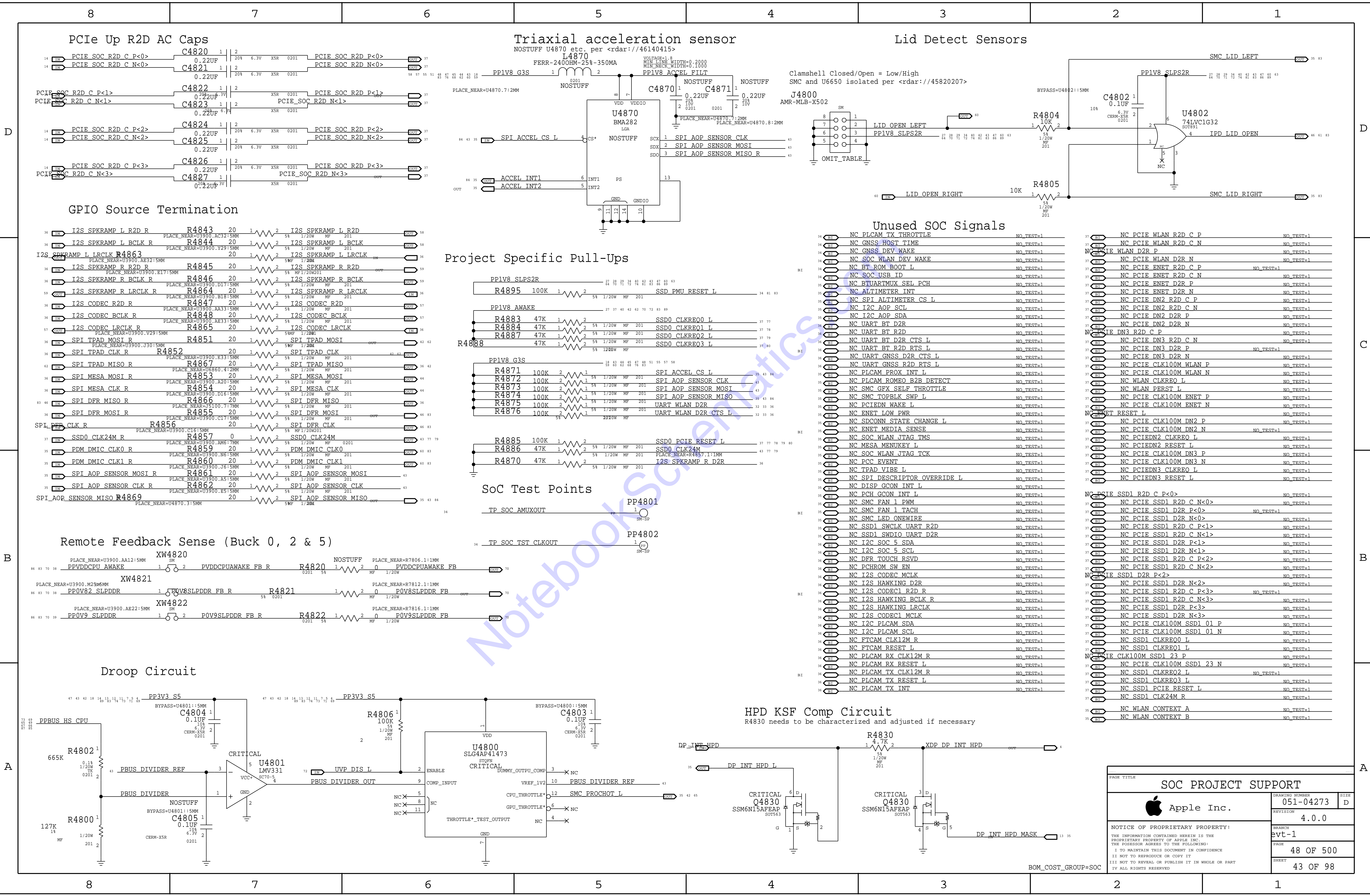
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	PAGE	45 OF 500
	SHEET	40 OF 98

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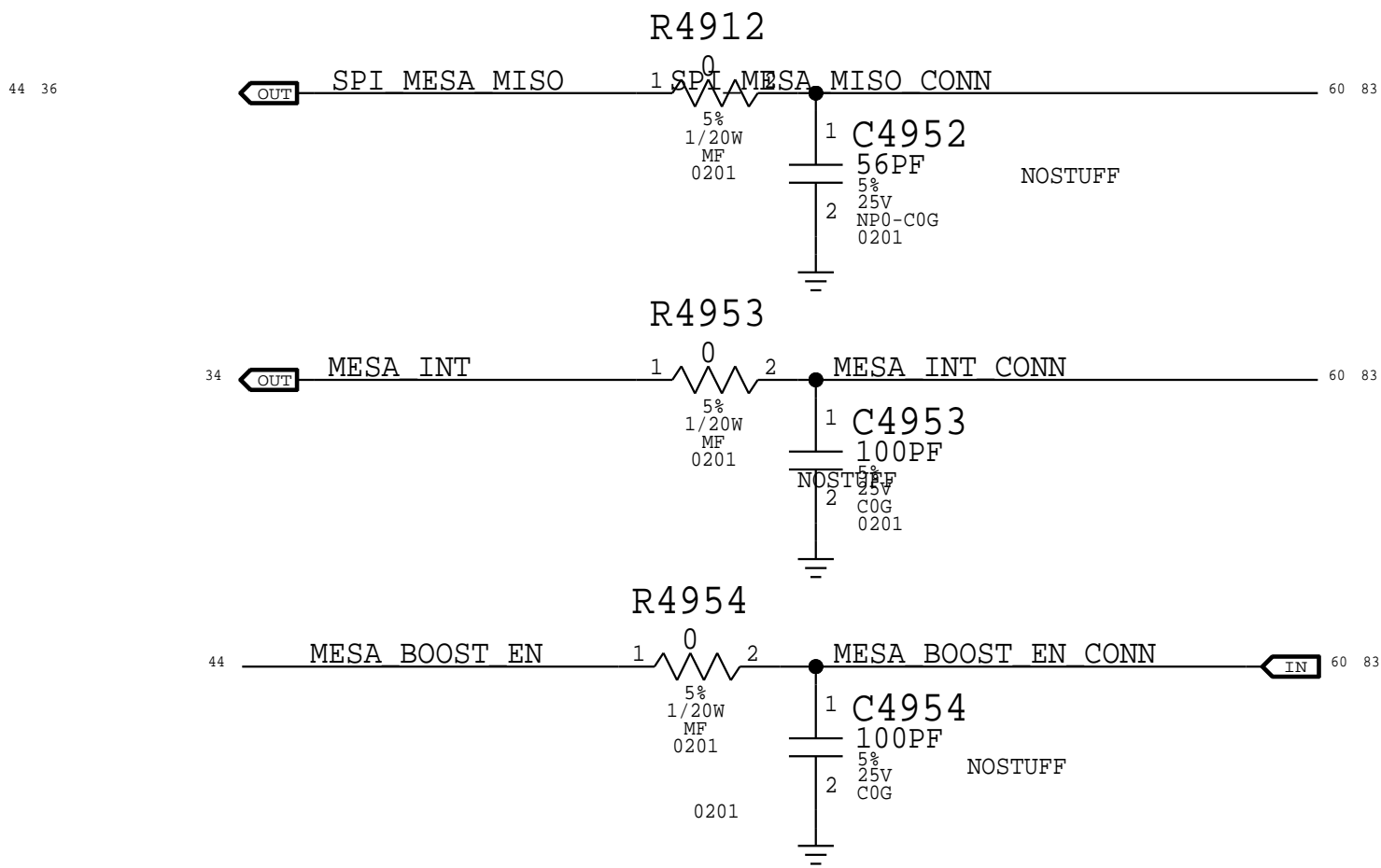
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	PAGE	46 OF 500
	SHEET	41 OF 98

BOM_COST_GROUP=SOC



ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

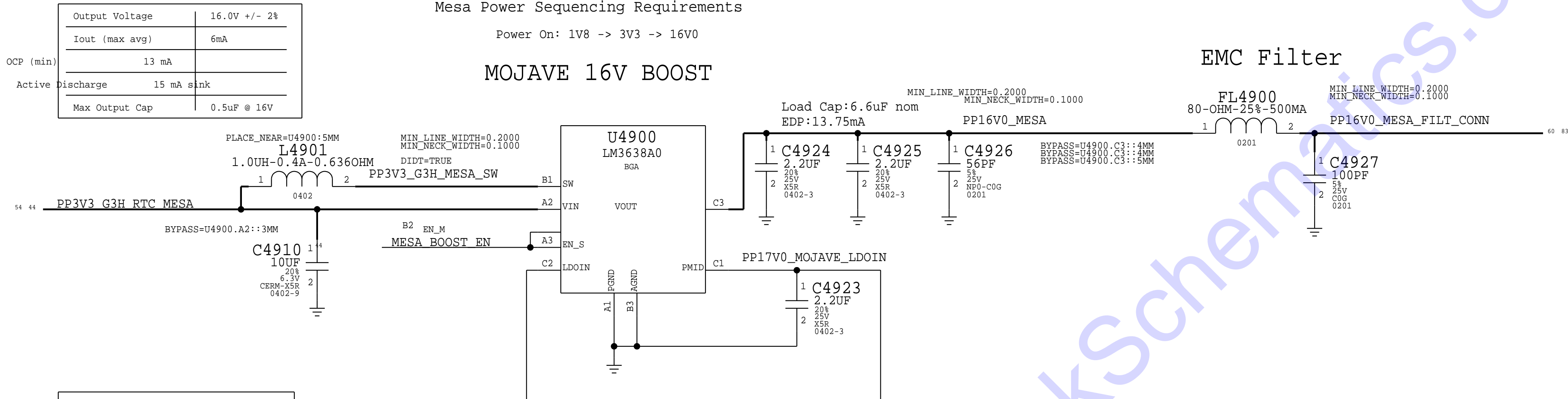
ESD Filters



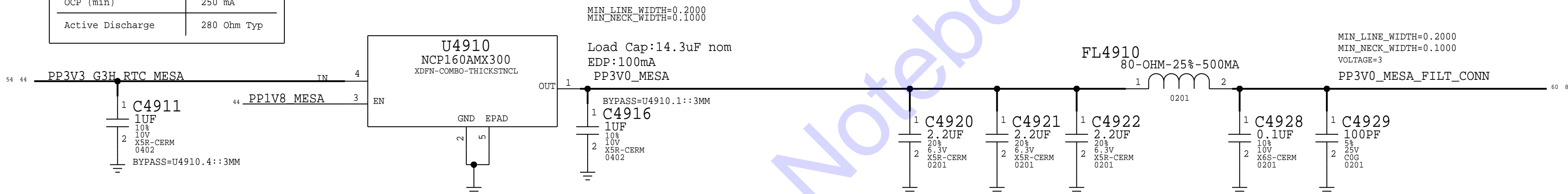
Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

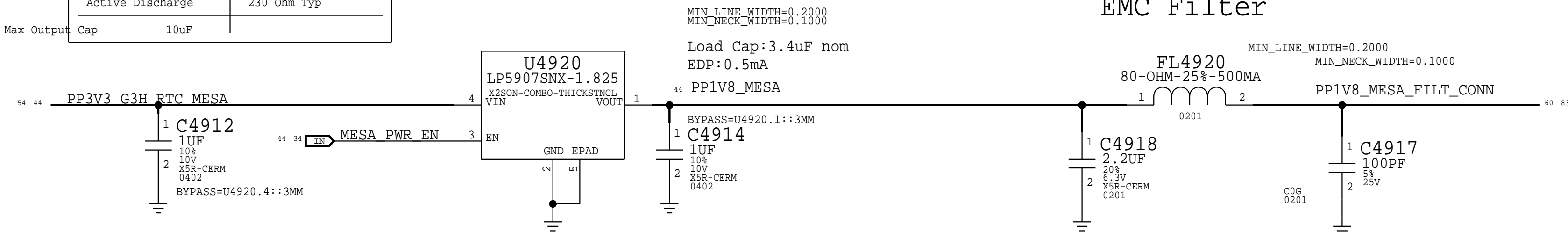
MOJAVE 16V BOOST



3.0V MESA



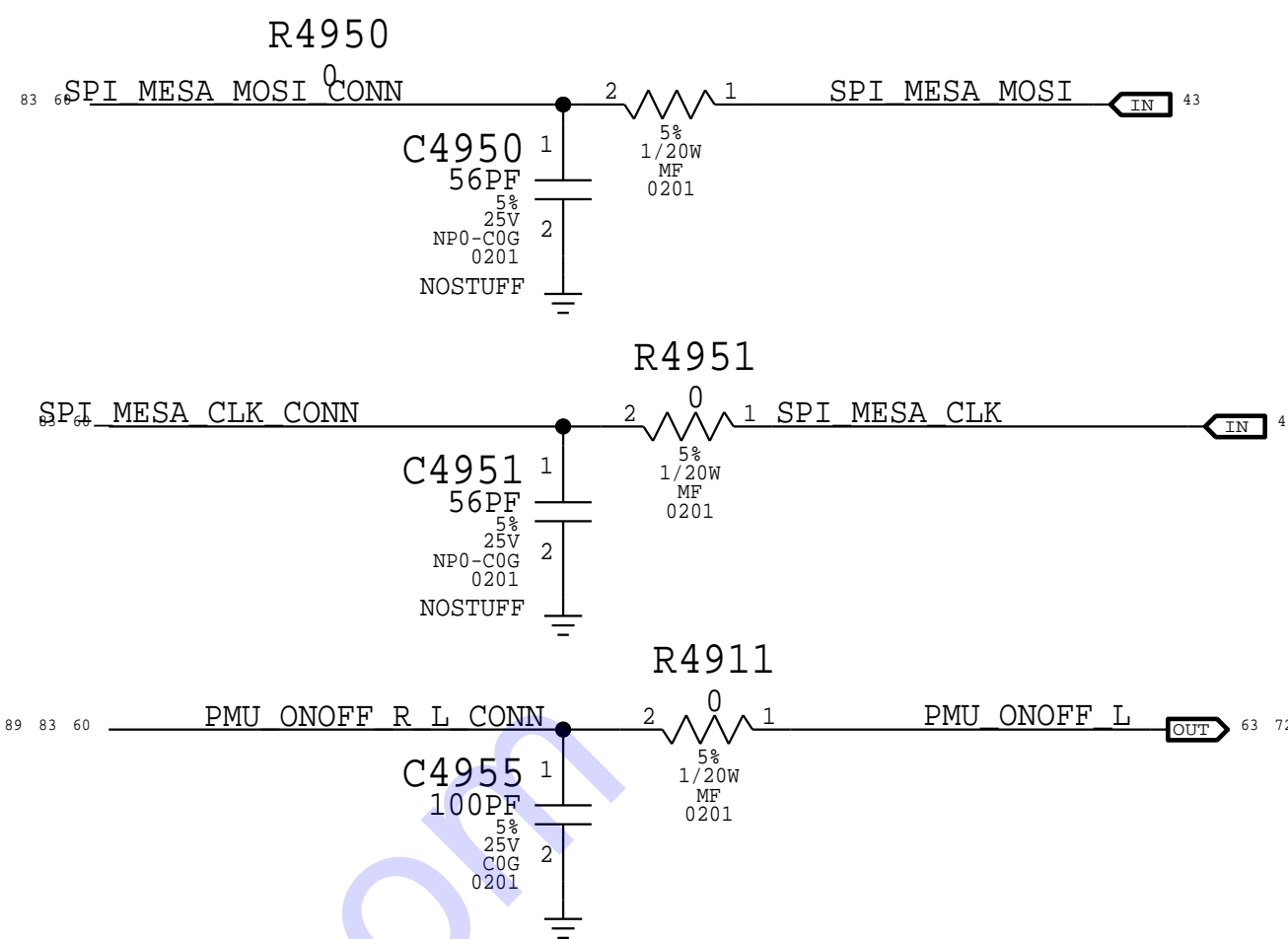
1.8V MESA



T151 FLEX CONNECTOR

ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

ESD Filters



EMC Filter

EMC Filter

EMC Filter

BOM_COST_GROUP=MESA

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T151		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	49 OF 500
		SHEET
		44 OF 98

D

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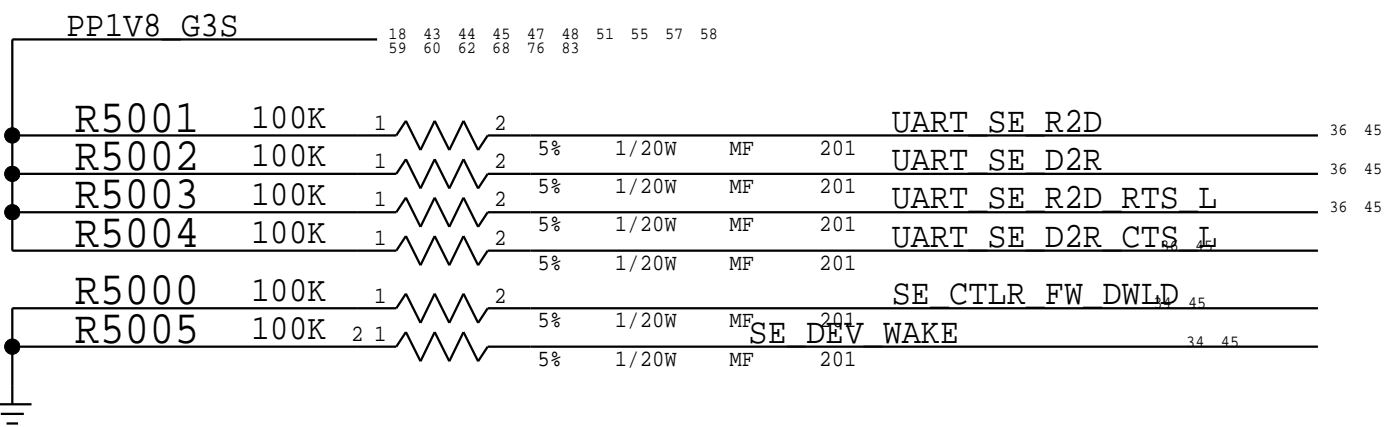
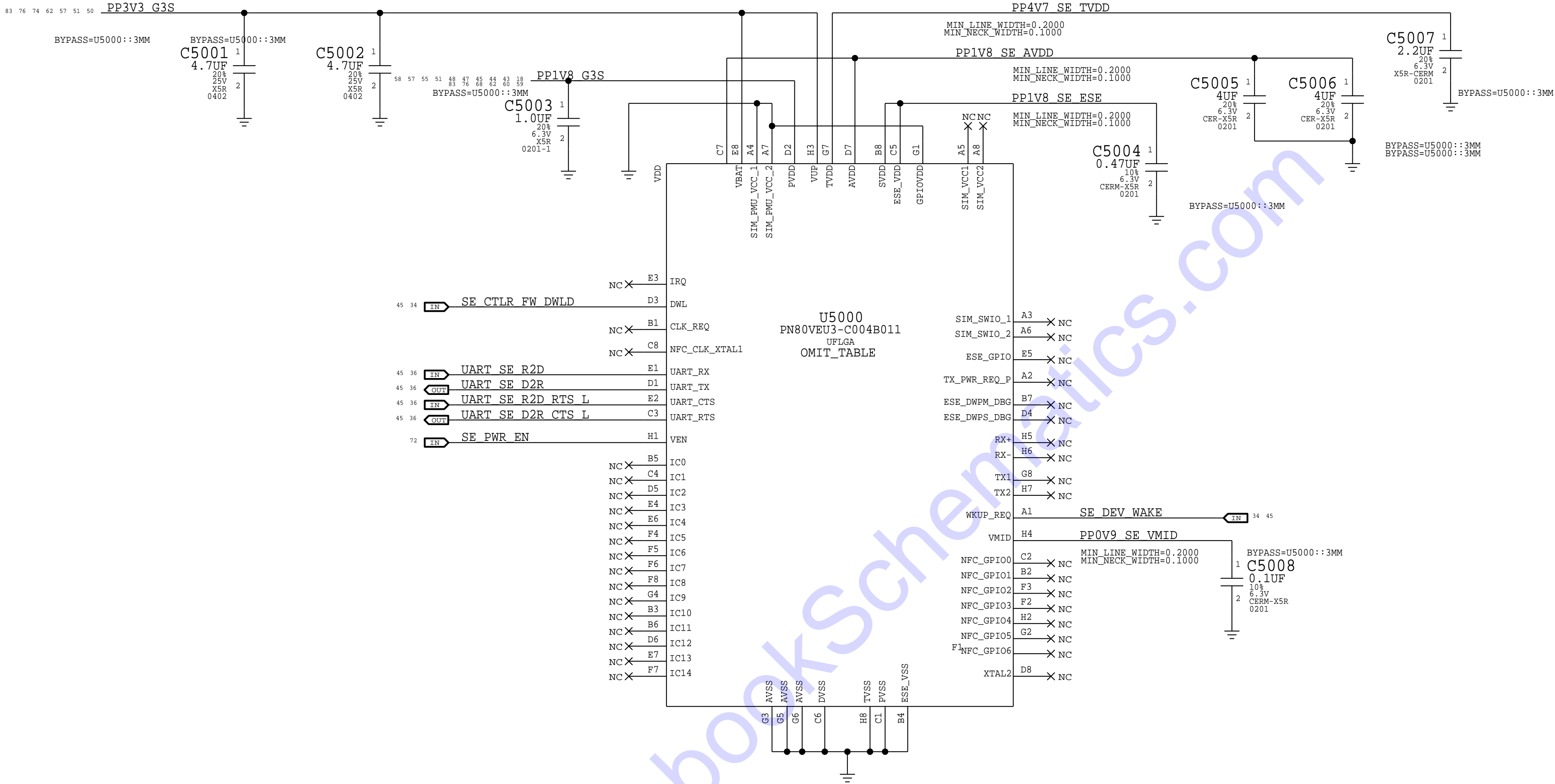
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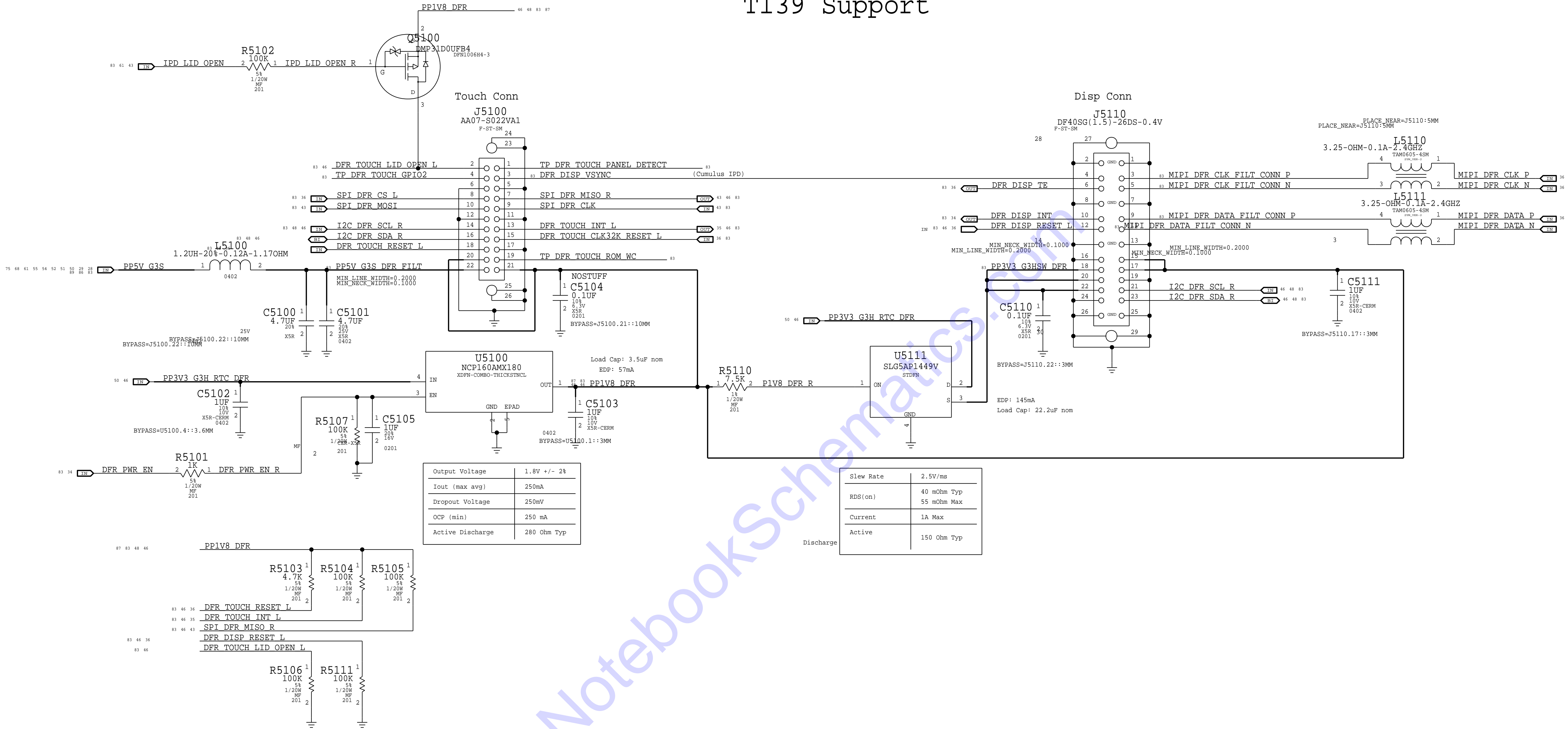
STOCKHOLM



BOM_COST_GROUP=SOC

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Secure Element		
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	REVISION	4.0.0
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	PAGE	50 OF 500
	SHEET	45 OF 98

T139 Support

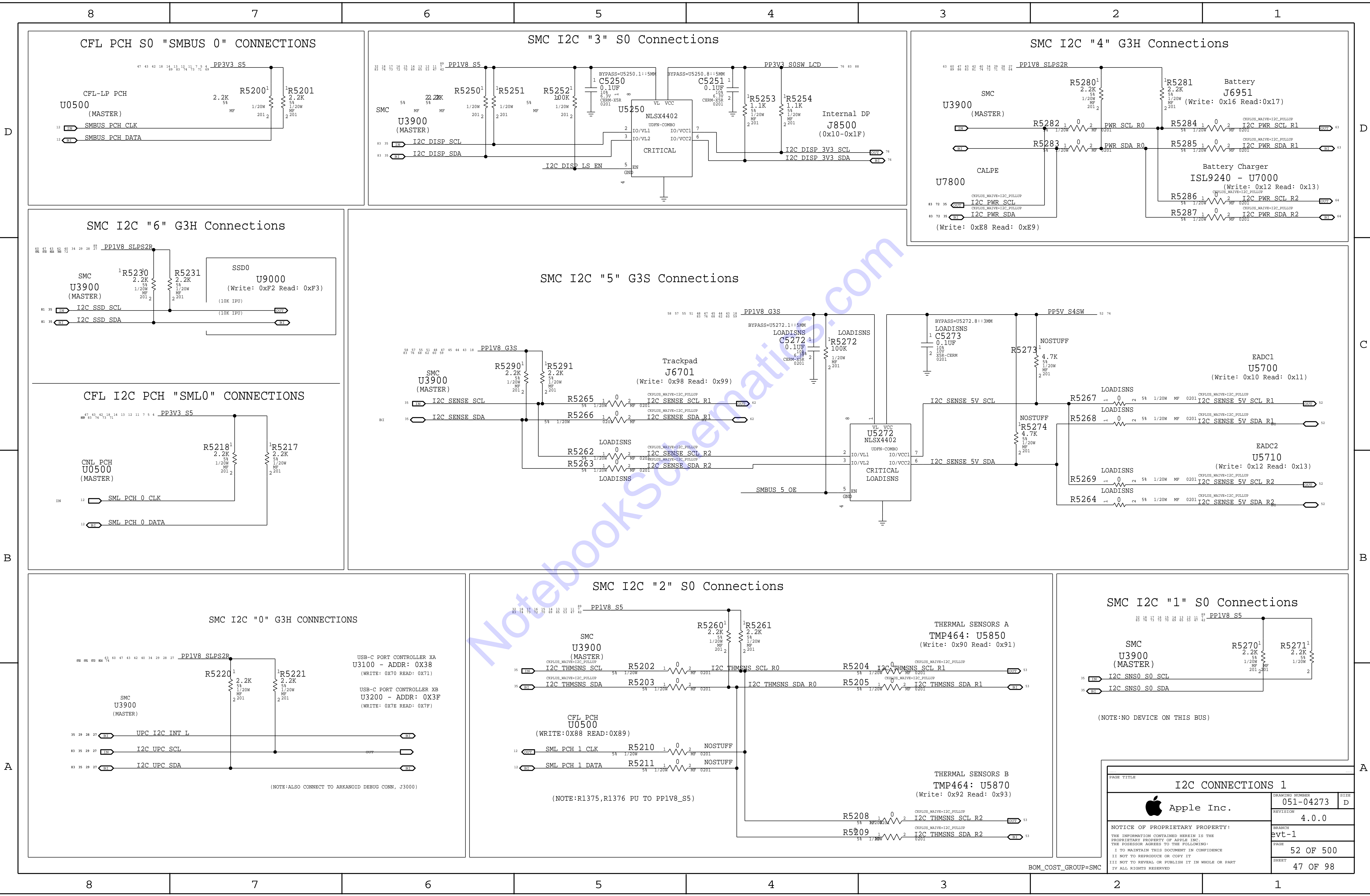


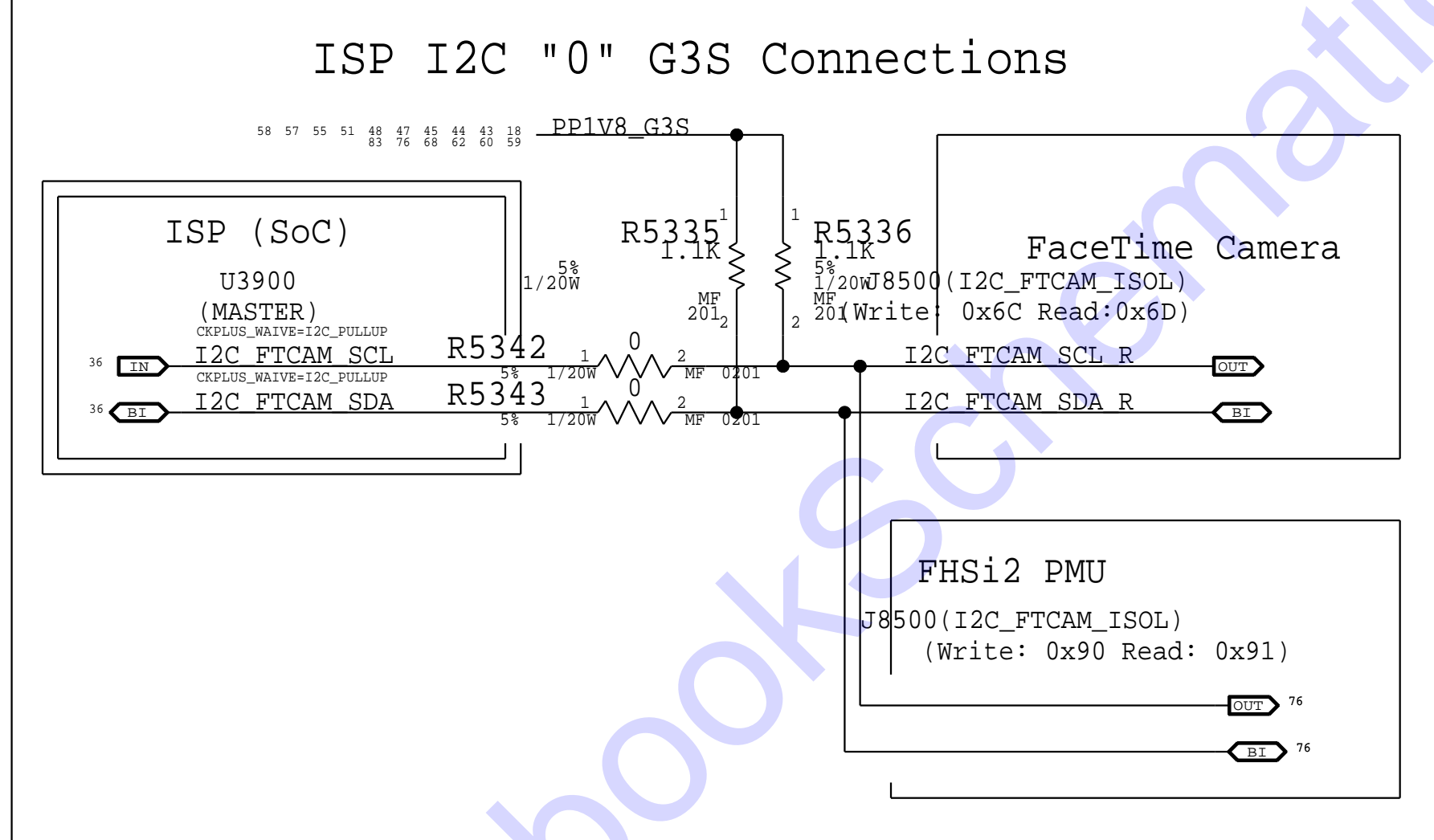
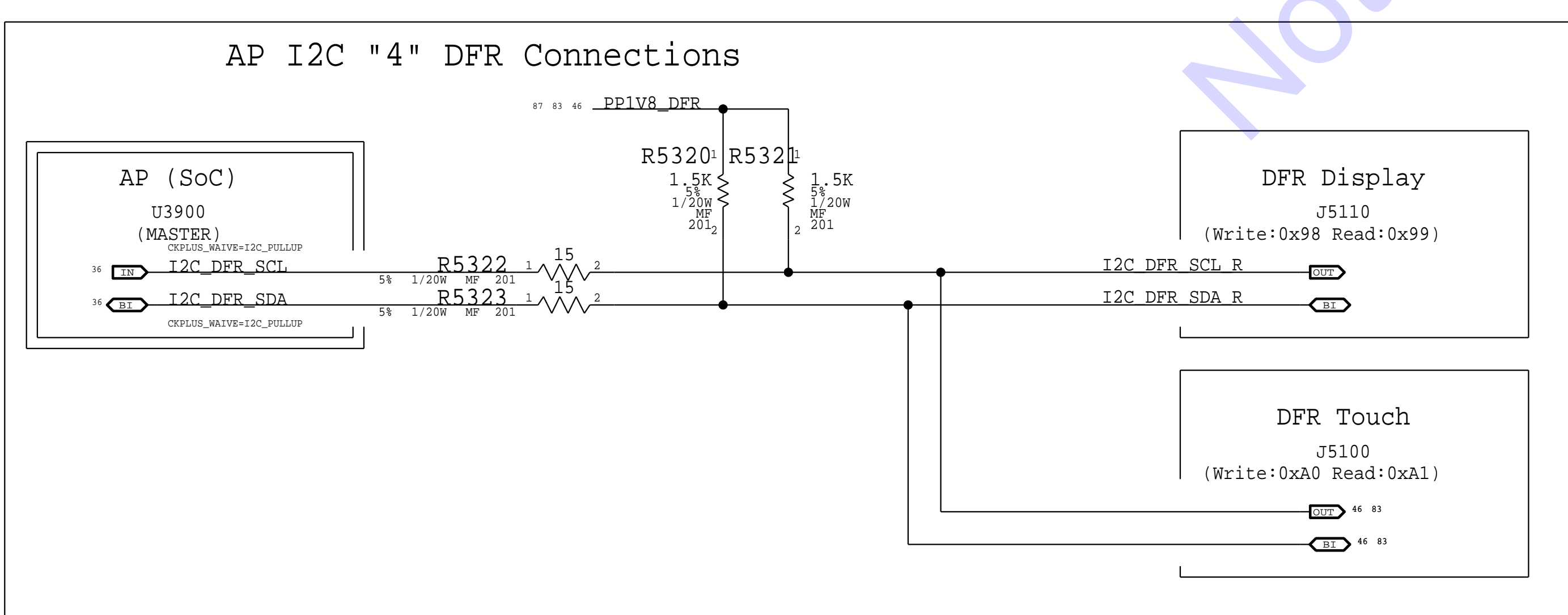
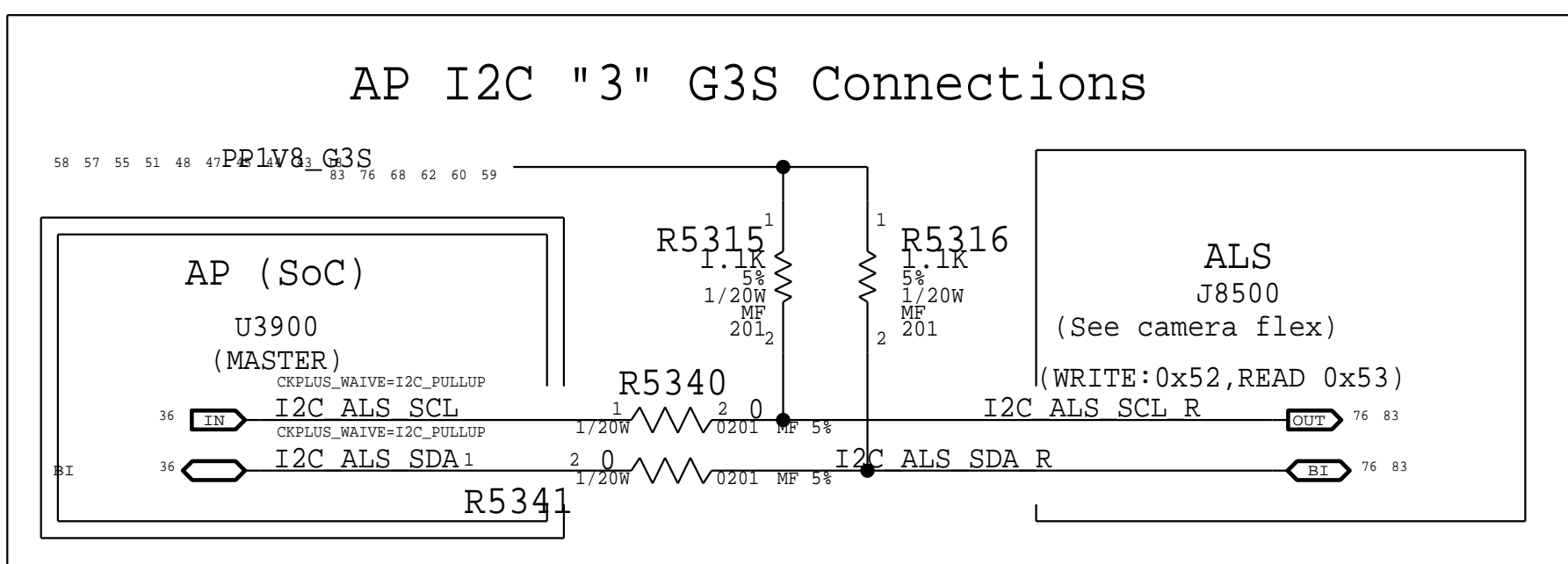
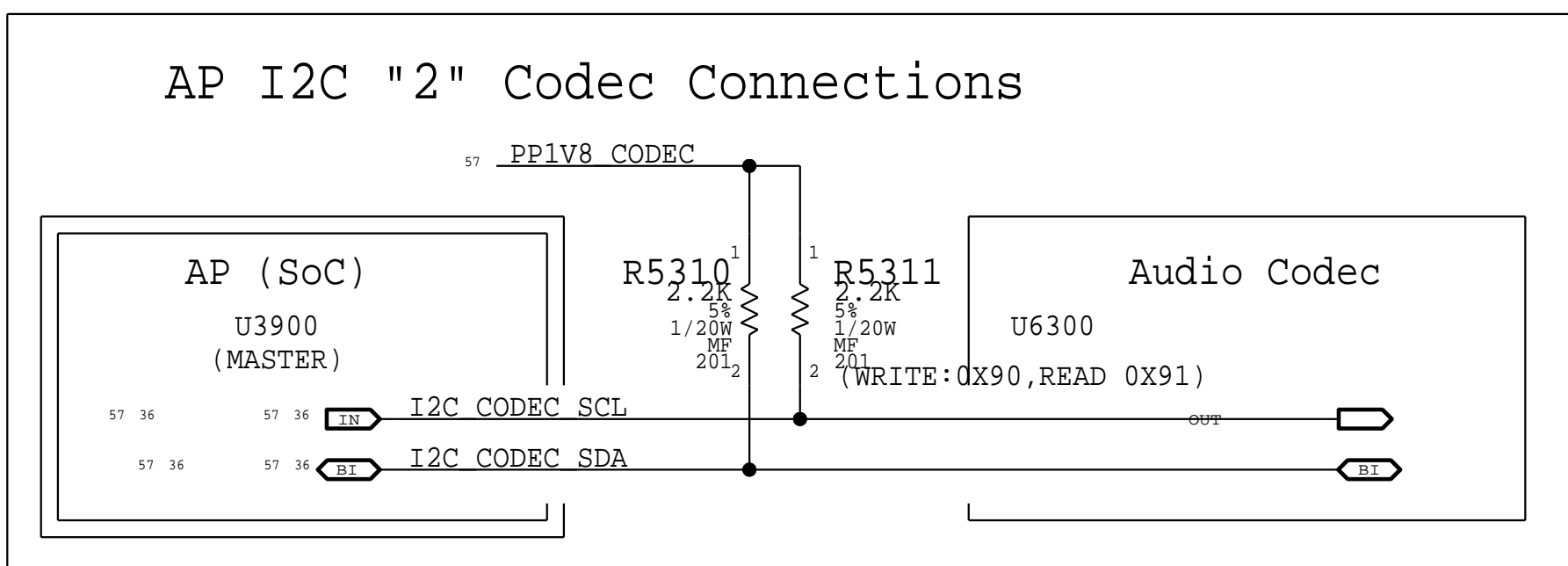
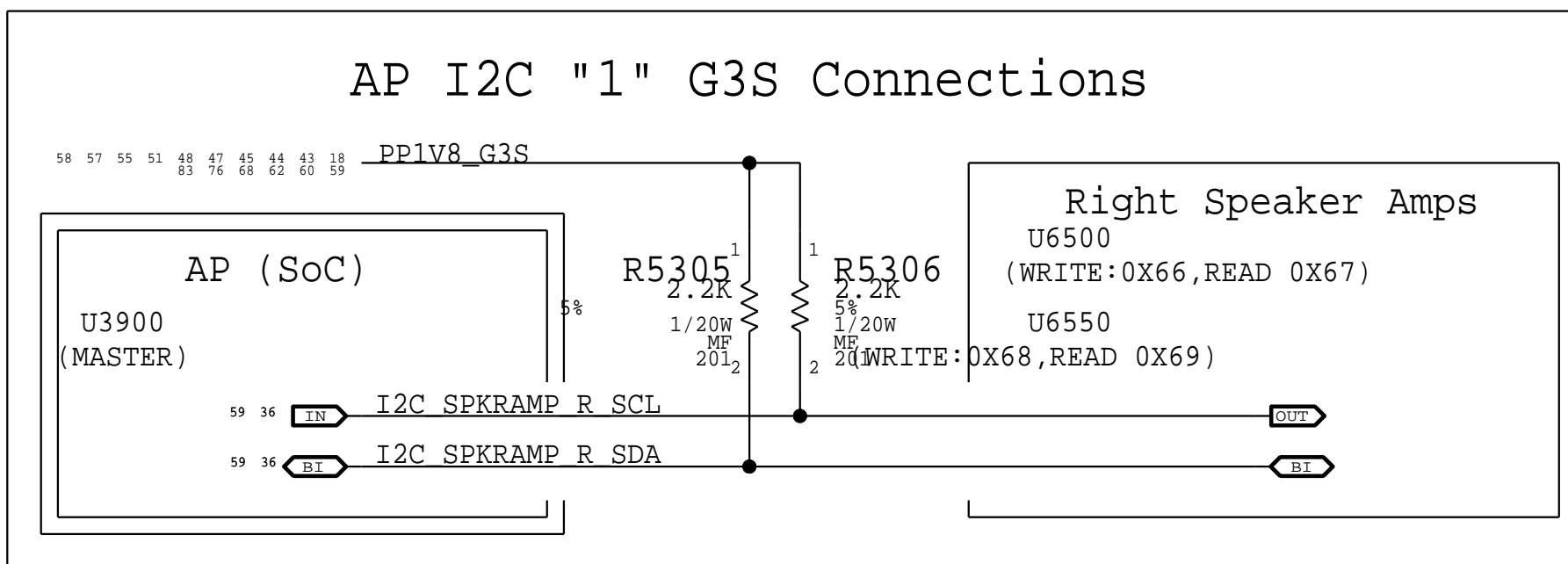
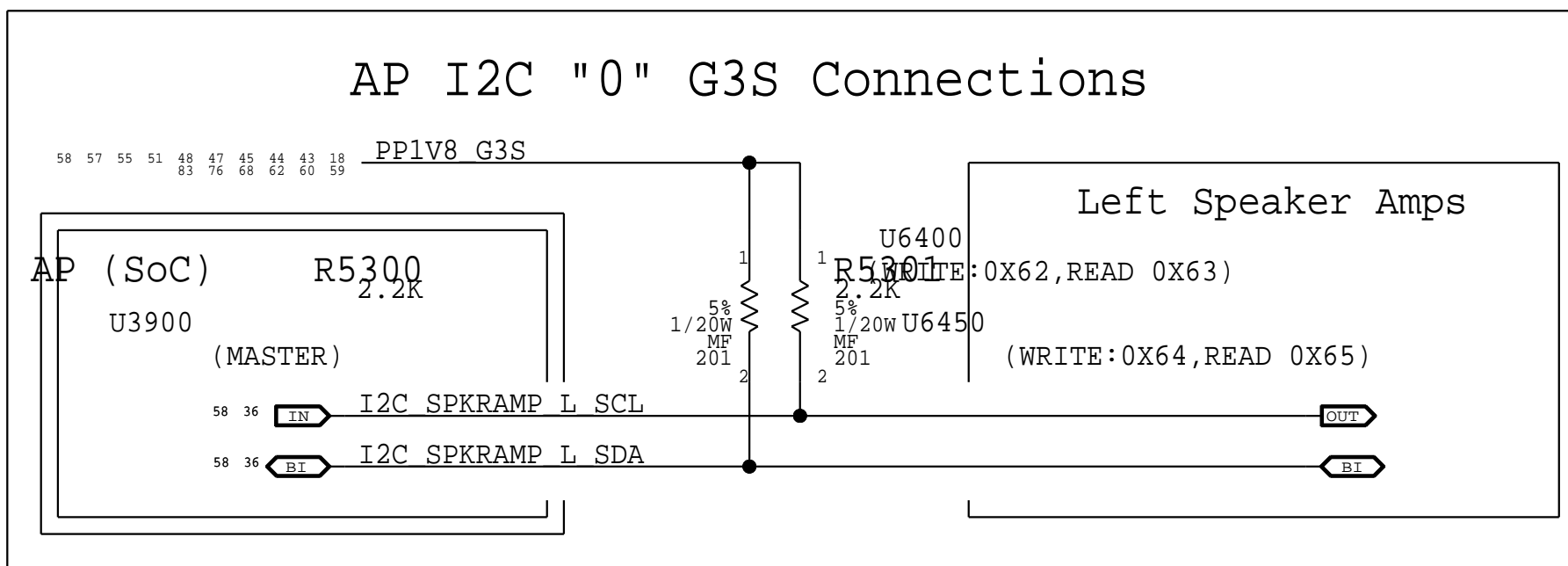
Output Voltage	1.8V +/- 2%
Iout (max avg)	250mA
Dropout Voltage	250mV
OCV (min)	250 mA
Active Discharge	280 Ohm Typ

Slew Rate	2.5V/ms
RDS(on)	40 mOhm Typ 55 mOhm Max
Current	1A Max
Active	150 Ohm Typ


PAGE TITLE		
T139 SUPPORT		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	51 OF 500
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BOM_COST_GROUP=DFR



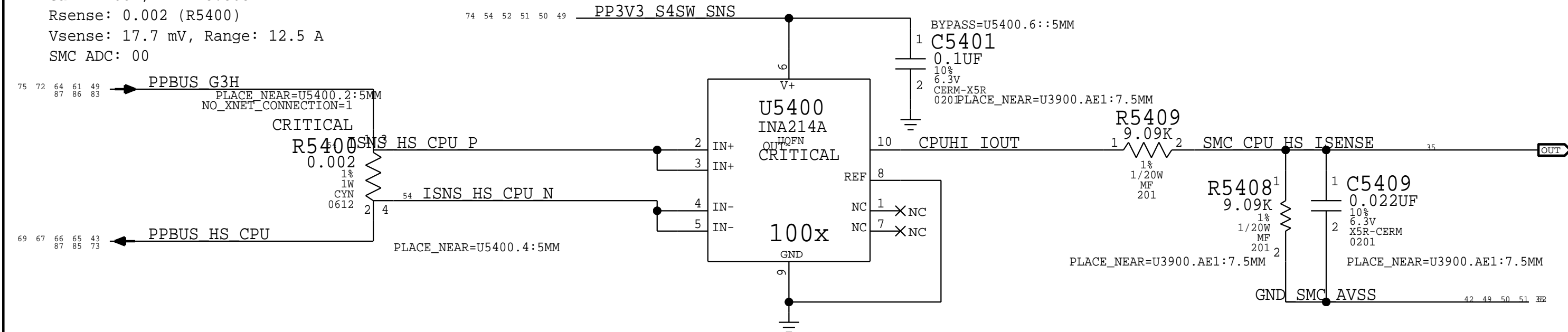


Device	SMC IF	ADDR. (8b)
ACE XA	I2C0	0X70/1
ACE XB	I2C0	0X7E/F
NC.	I2C1	
TEMP. SENSOR A	I2C2	0X90/1
TEMP. SENSOR B	I2C2	0X92/3
TCON	I2C3	0X10-1F
Charger	I2C4	0X12/3
Battery	I2C4	0X16/7
Calpe	I2C4	0XE8/9
Trackpad	I2C5	0X98/9
EADC1	I2C5	0X10/1
EADC2	I2C5	0X12/3
SSD	I2C6	0XF2/3
SOC IF (AP)		
Left Spkr Amp.(U6400)	I2C0	0X62/3
Left Spkr Amp.(U6450)	I2C0	0X64/5
Right Spkr Amp.(U6500)	I2C1	0X66/7
Right Spkr Amp.(U6550)	I2C1	0X68/9
Audio Codec	I2C2	0X90/1
ALS	I2C3	0X52/3
DFR Display	I2C4	0X98/9
DFR Touch	I2C4	0XA0/1
NC.	I2C5	
Spkr ID1	I2C6	
Spkr ID0	I2C6	
SIP IF (ISP)		
FT Camera	I2C0	0X6C/D
FHSi2	I2C0	0X90/1
NC.	I2C1	
AOP IF		
NC.	I2C0	

PAGE TITLE			
I2C CONNECTIONS 2			
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IV ALL RIGHTS RESERVED		48 OF 98	

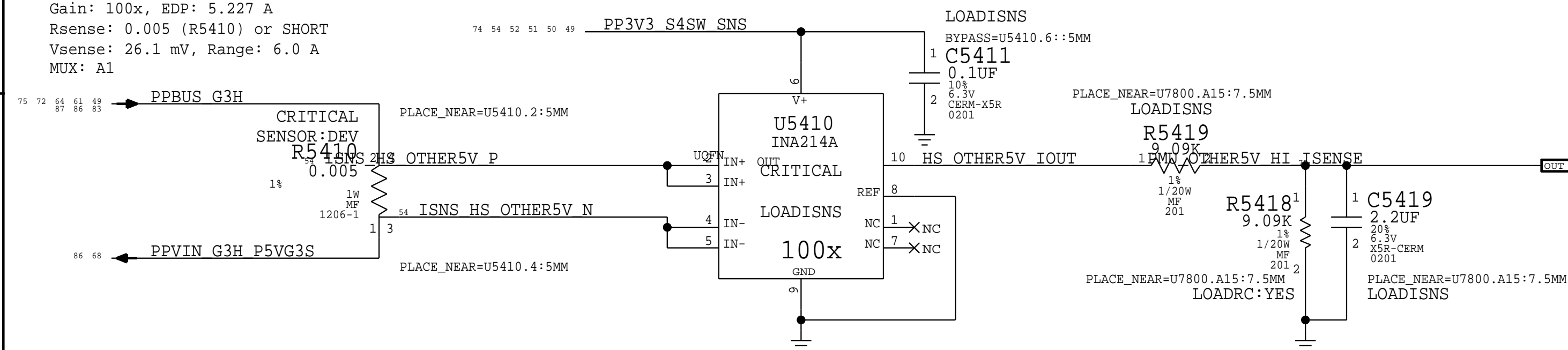
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 8.868 A
Rsense: 0.002 (R5400)
Vsense: 17.7 mV, Range: 12.5 A
SMC ADC: 00



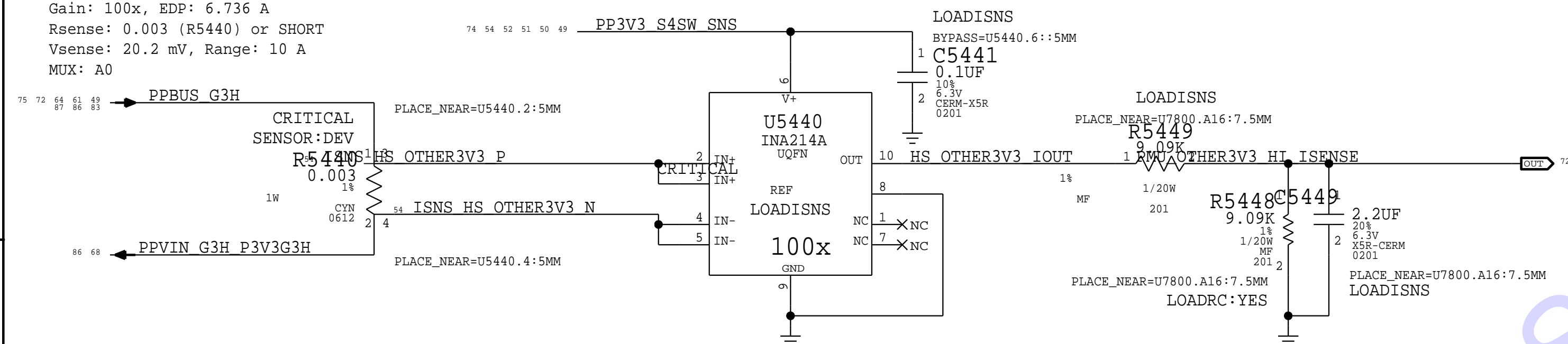
OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 5.227 A
Rsense: 0.005 (R5410) or SHORT
Vsense: 26.1 mV, Range: 6.0 A
MUX: A1



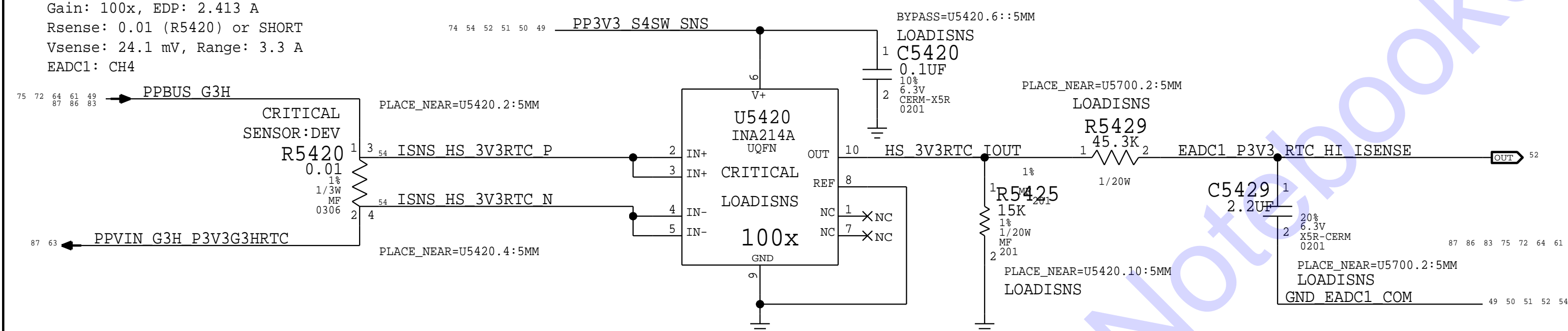
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 100x, EDP: 6.736 A
Rsense: 0.003 (R5440) or SHORT
Vsense: 20.2 mV, Range: 10 A
MUX: A0



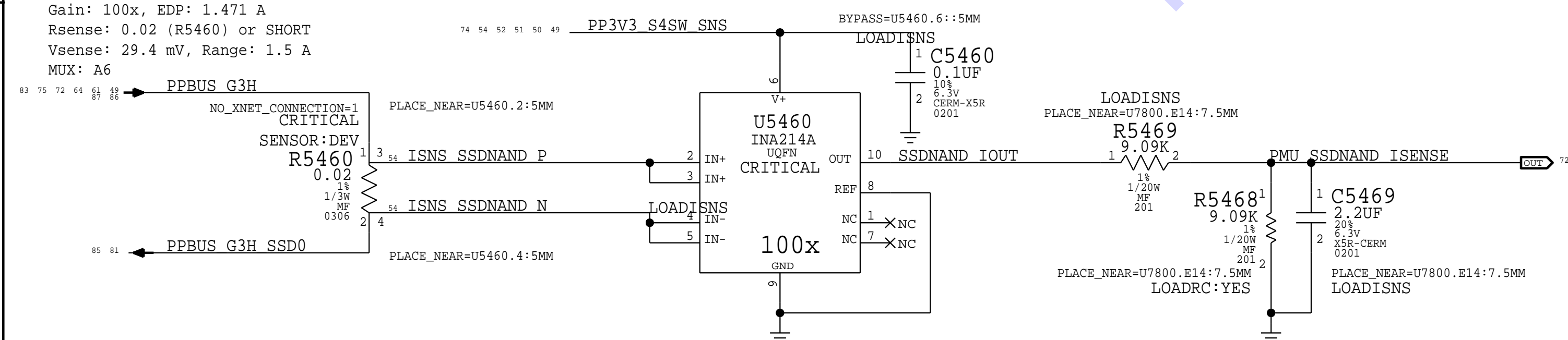
3.3V RTC High Side Current Sense (IR3R)

Gain: 100x, EDP: 2.413 A
Rsense: 0.01 (R5420) or SHORT
Vsense: 24.1 mV, Range: 3.3 A
EADC1: CH4



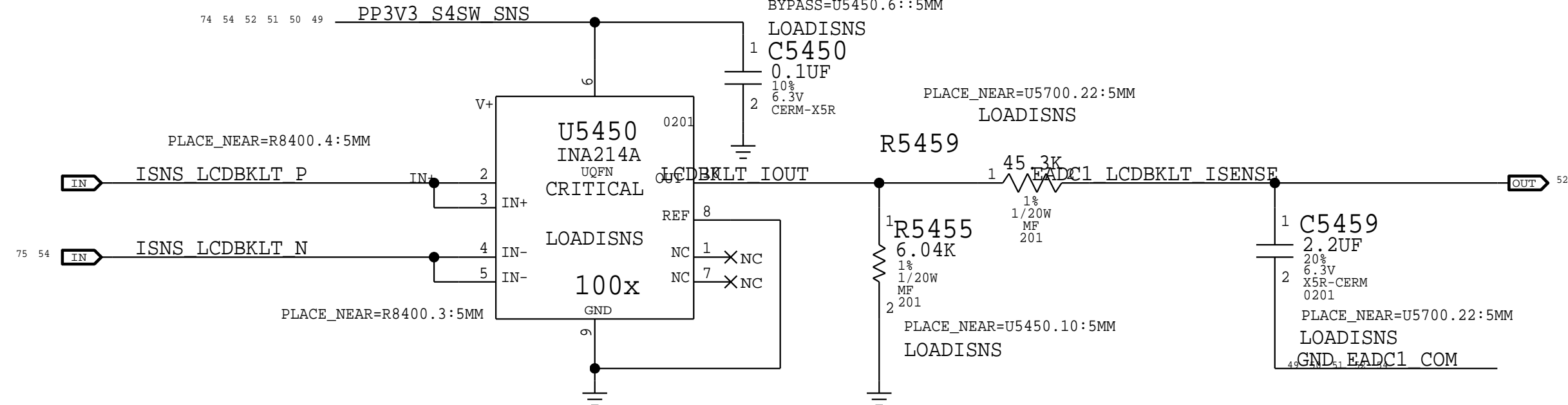
NAND Current Sense (IHNR)

Gain: 100x, EDP: 1.471 A
Rsense: 0.02 (R5460) or SHORT
Vsense: 29.4 mV, Range: 1.5 A
MUX: A6



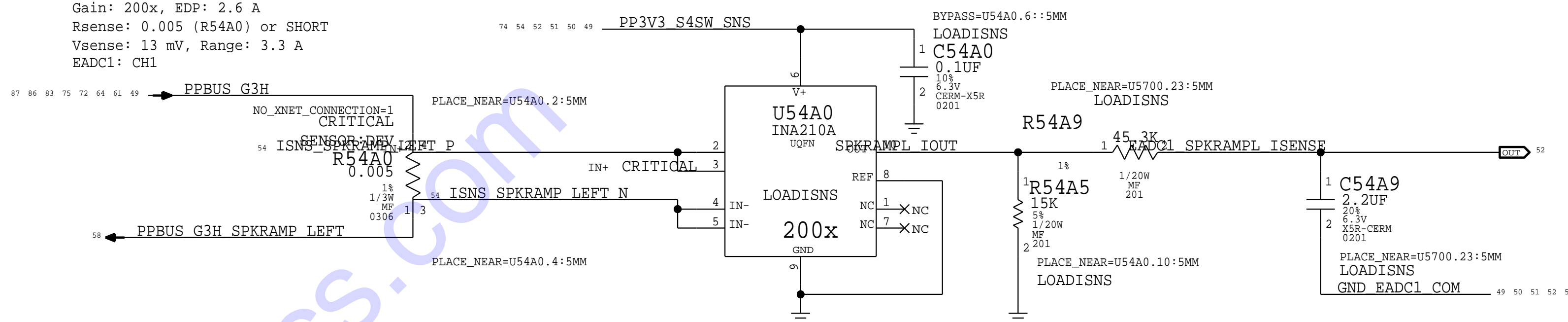
LCD Backlight Current Sense (IBLR)

Gain: 100x, EDP: 0.902 A
Rsense: 0.025 (R8400)
Vsense: 22.6 mV, Range: 1.32 A
EADC1: CH0



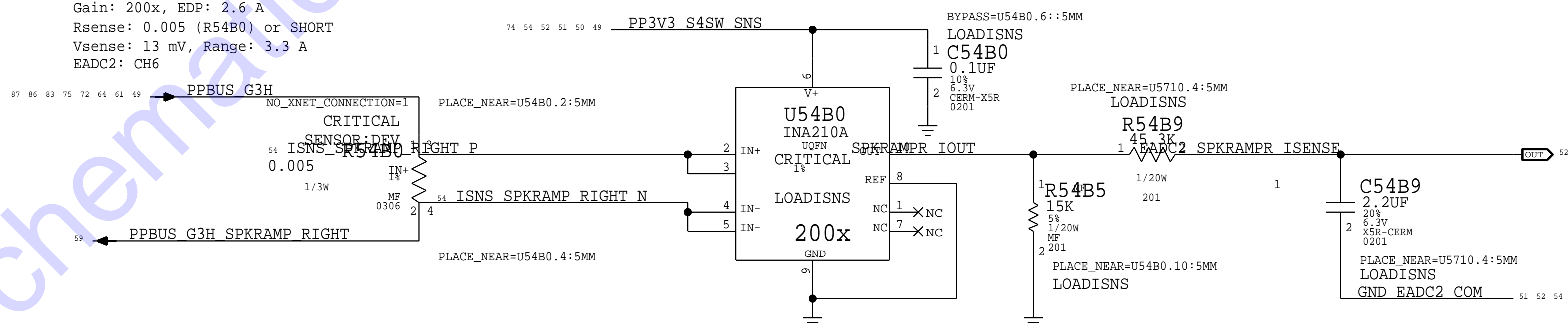
Left AMP Current Sense (IALR)

Gain: 200x, EDP: 2.6 A
Rsense: 0.005 (R54A0) or SHORT
Vsense: 13 mV, Range: 3.3 A
EADC1: CH1



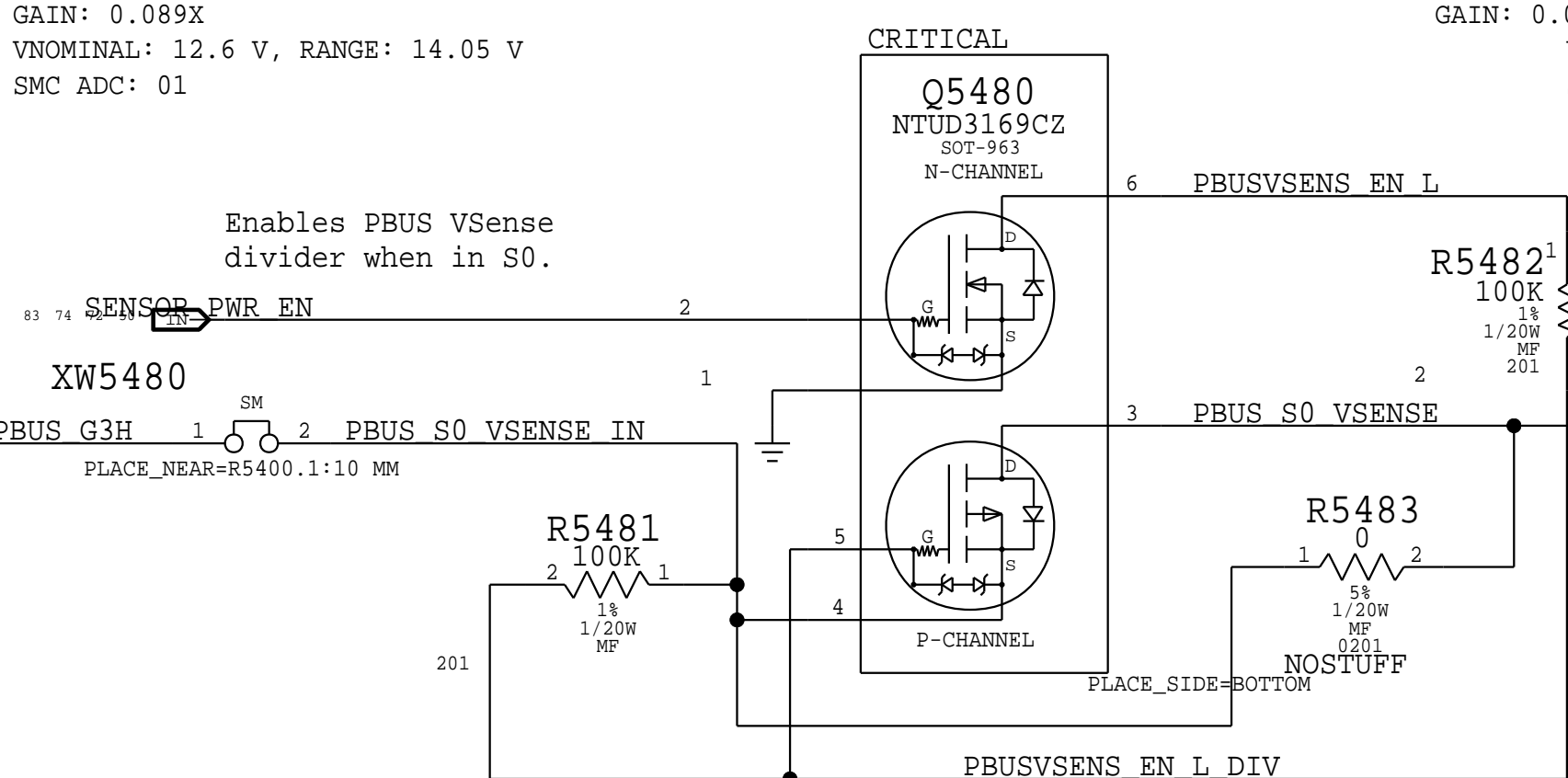
Right AMP Current Sense (IARR)

Gain: 200x, EDP: 2.6 A
Rsense: 0.005 (R54B0) or SHORT
Vsense: 13 mV, Range: 3.3 A
EADC2: CH6



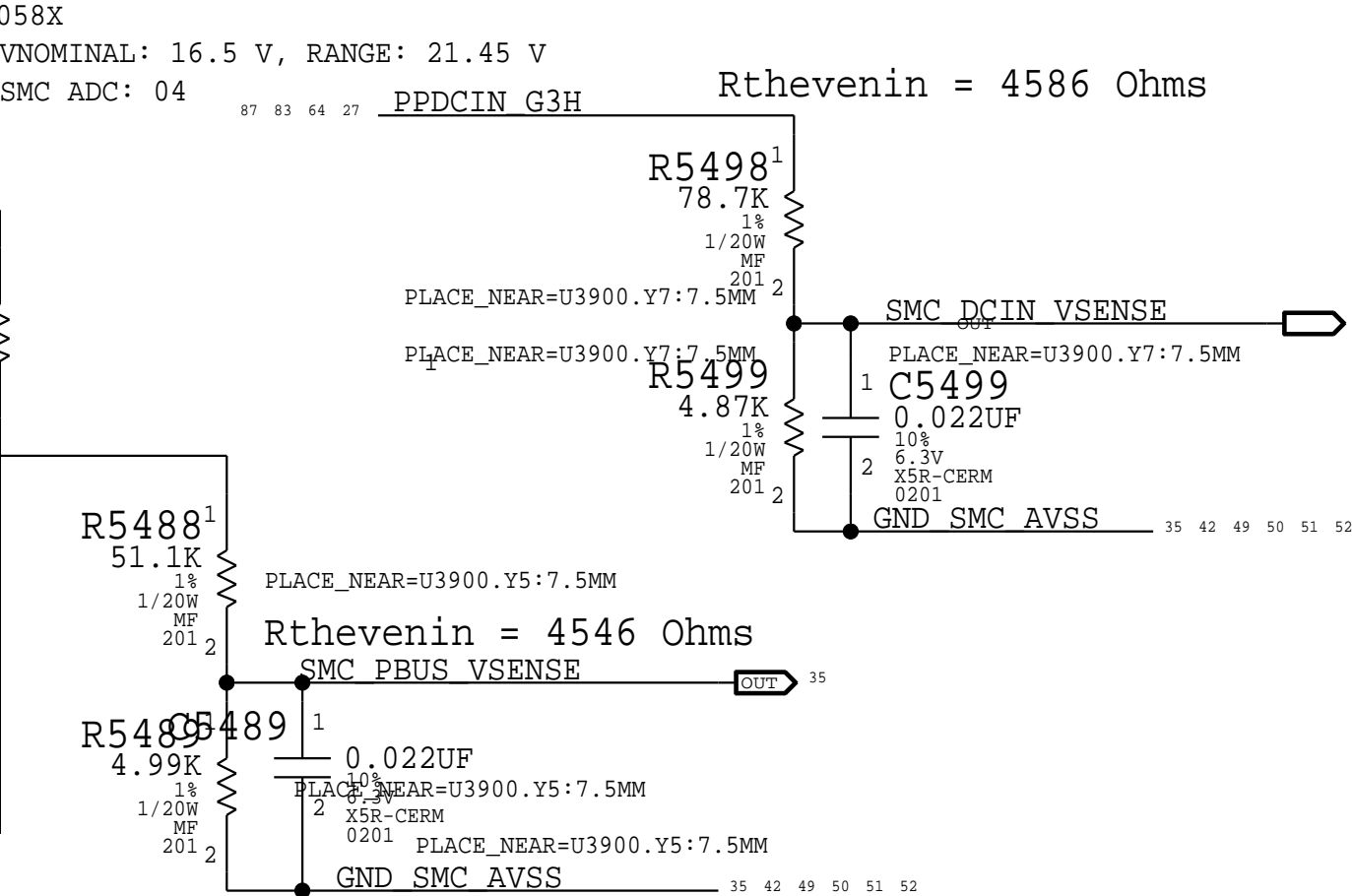
PBUS Voltage Sense & Enable (VP0R)

GAIN: 0.089X
VNOMINAL: 12.6 V, RANGE: 14.05 V
SMC ADC: 01



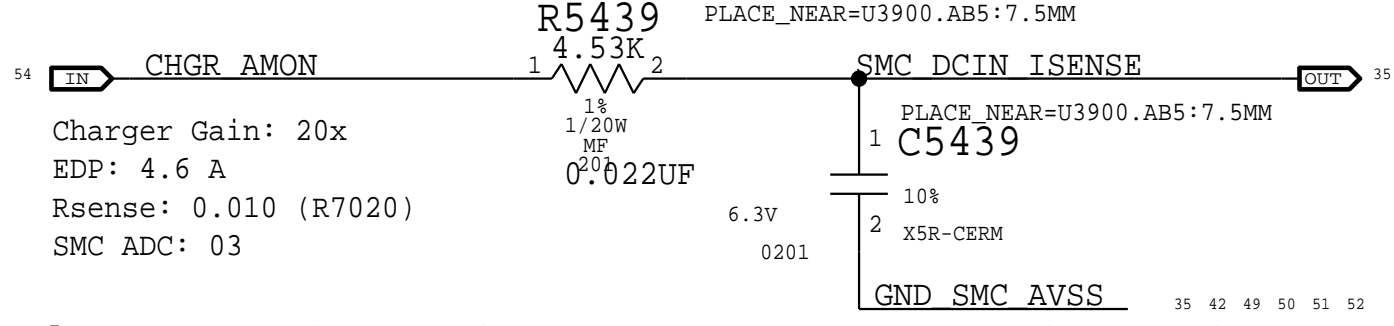
DC In Voltage Sense (VD0R)

GAIN: 0.058X
VNOMINAL: 16.5 V, RANGE: 21.45 V
SMC ADC: 04



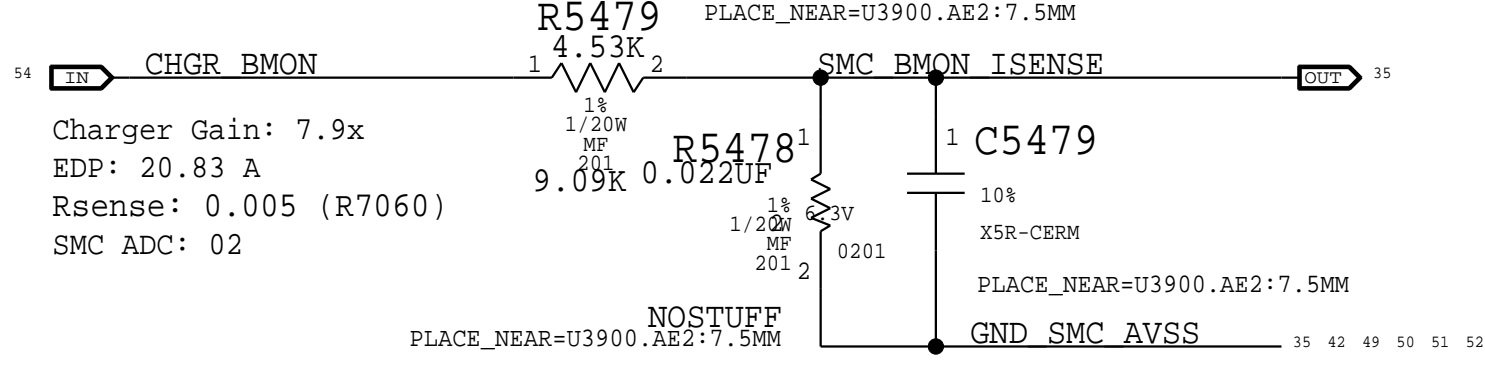
DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x
EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 03



Charger (BMON) Current Sense (IPBR)

Charger Gain: 7.9x
EDP: 20.83 A
Rsense: 0.005 (R7060)
SMC ADC: 02



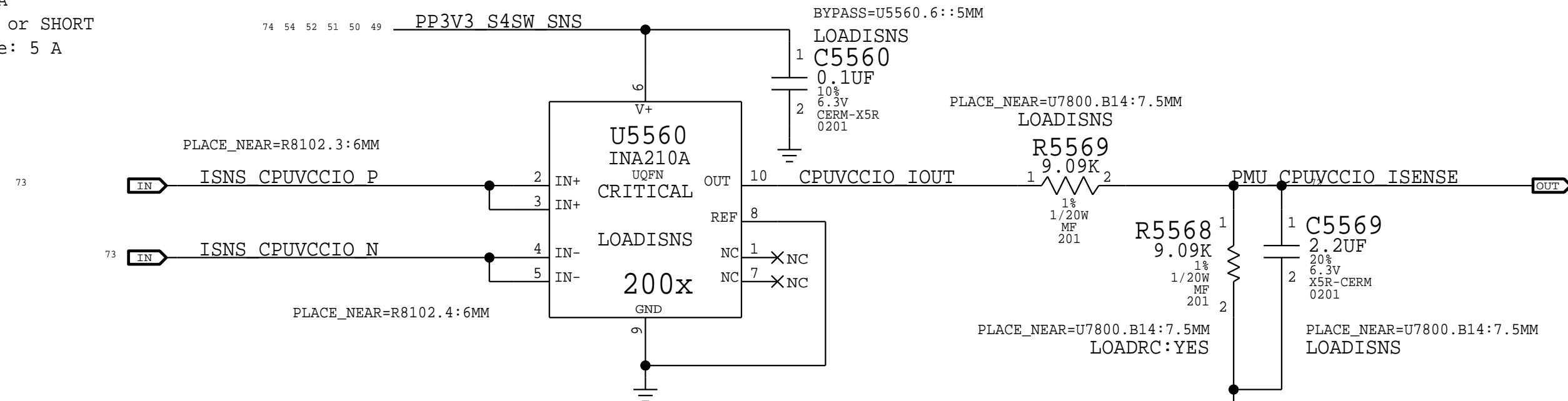
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	R5418,R5448,R5478		LOADRC:NO

PAGE TITLE			POWER SENSORS HIGH SIDE	
Apple Inc.		DRAWING NUMBER	051-04273	SIZE
		REVISION	4.0.0	D
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BOM_COST_GROUP=SENSORS

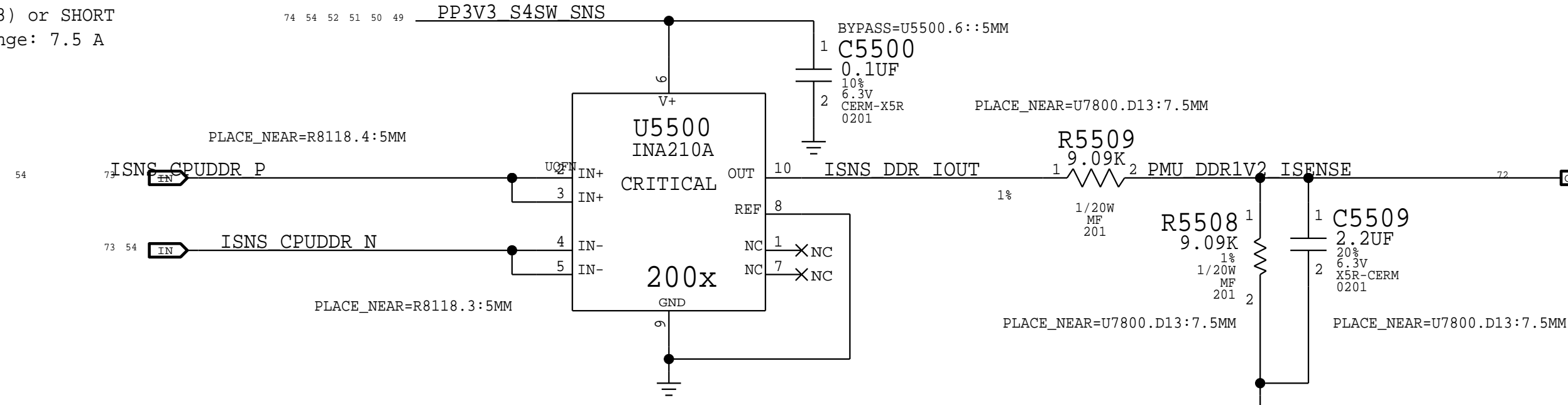
CPU VCCIO Current Sense (IC1C)

Gain: 200x, EDP: 3.6 A
Rsense: 0.003 (R8102) or SHORT
Vsense: 10.8 mV, Range: 5 A
PMU AMUX: A3



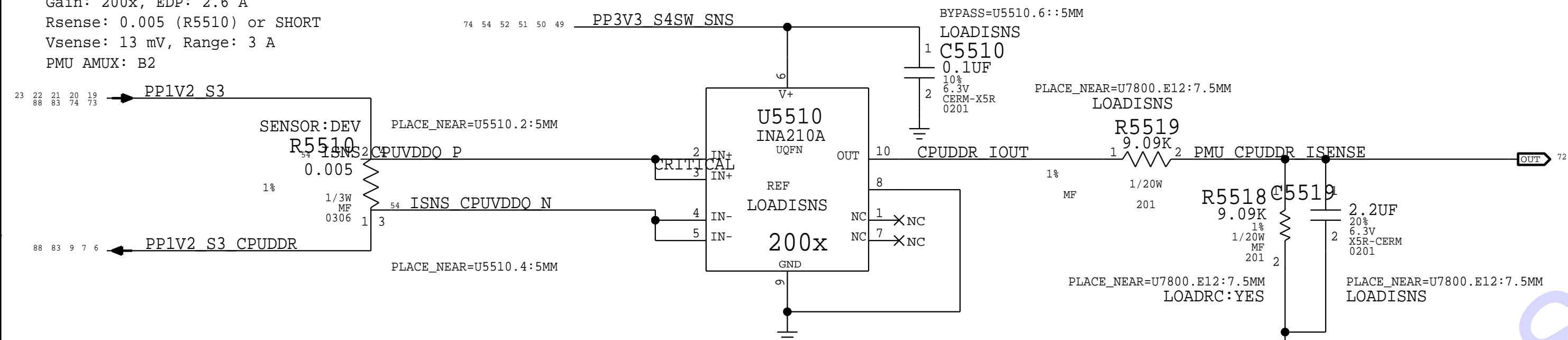
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 200x, EDP: 6.9 A
Rsense: 0.002 (R8118) or SHORT
Vsense: 13.8 mV, Range: 7.5 A
PMU AMUX: A4



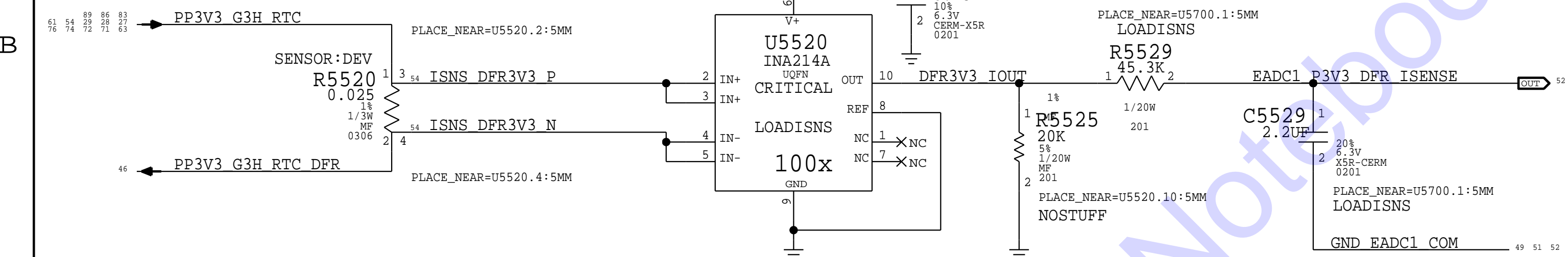
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2.6 A
Rsense: 0.005 (R5510) or SHORT
Vsense: 13 mV, Range: 3 A
PMU AMUX: B2



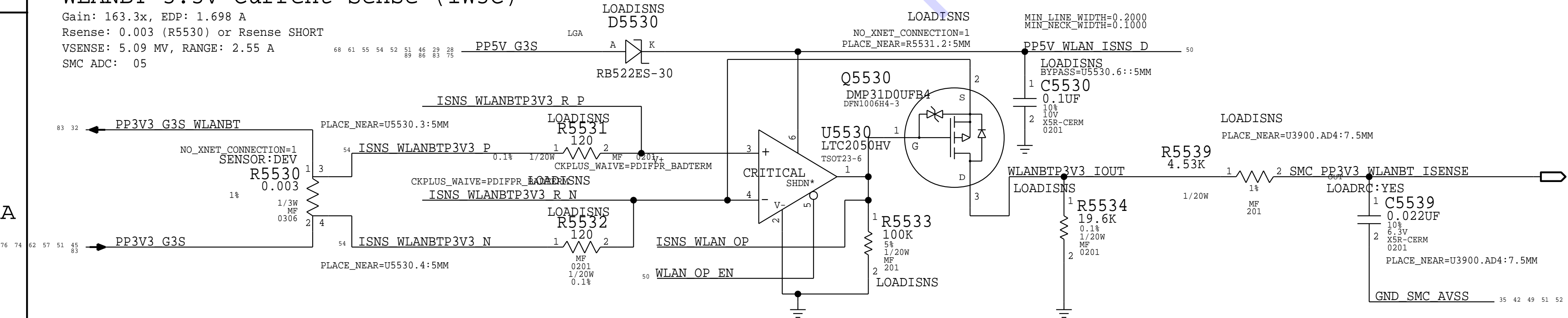
DFR Current Sense (IF3C)

Gain: 100x, EDP: 0.75 A
Rsense: 0.025 (R5520) or SHORT
Vsense: 18.8 mV, Range: 1.32 A
EADC1: CH3



WLANBT 3.3V Current Sense (IW3C)

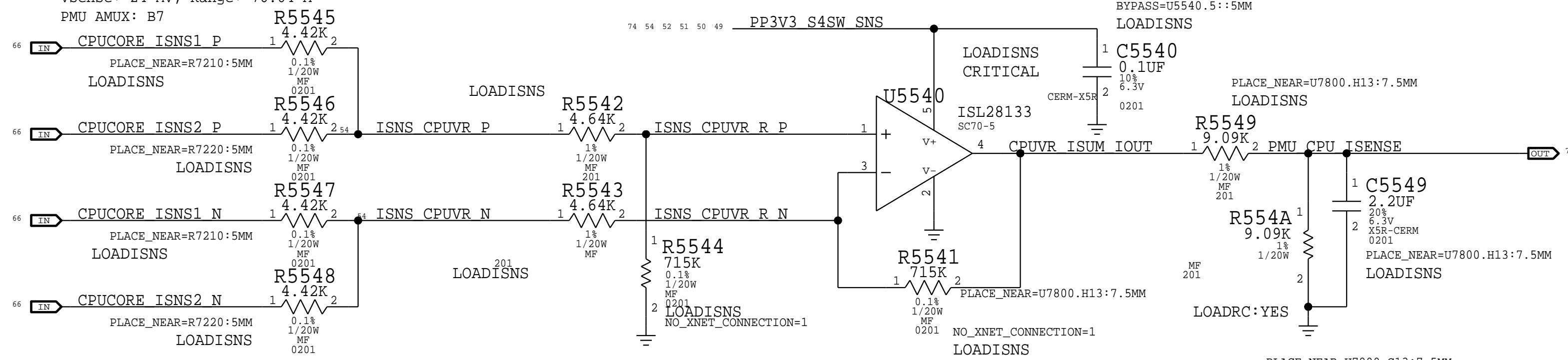
Gain: 163.3x, EDP: 1.698 A
Rsense: 0.003 (R5530) or Rsense SHORT
VSENSE: 5.09 mV, RANGE: 2.55 A
SMC ADC: 05



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FLIM,100K,1/16W,0201,SMD	R5518,R5568,R554A,C5539		LOADRC:NO

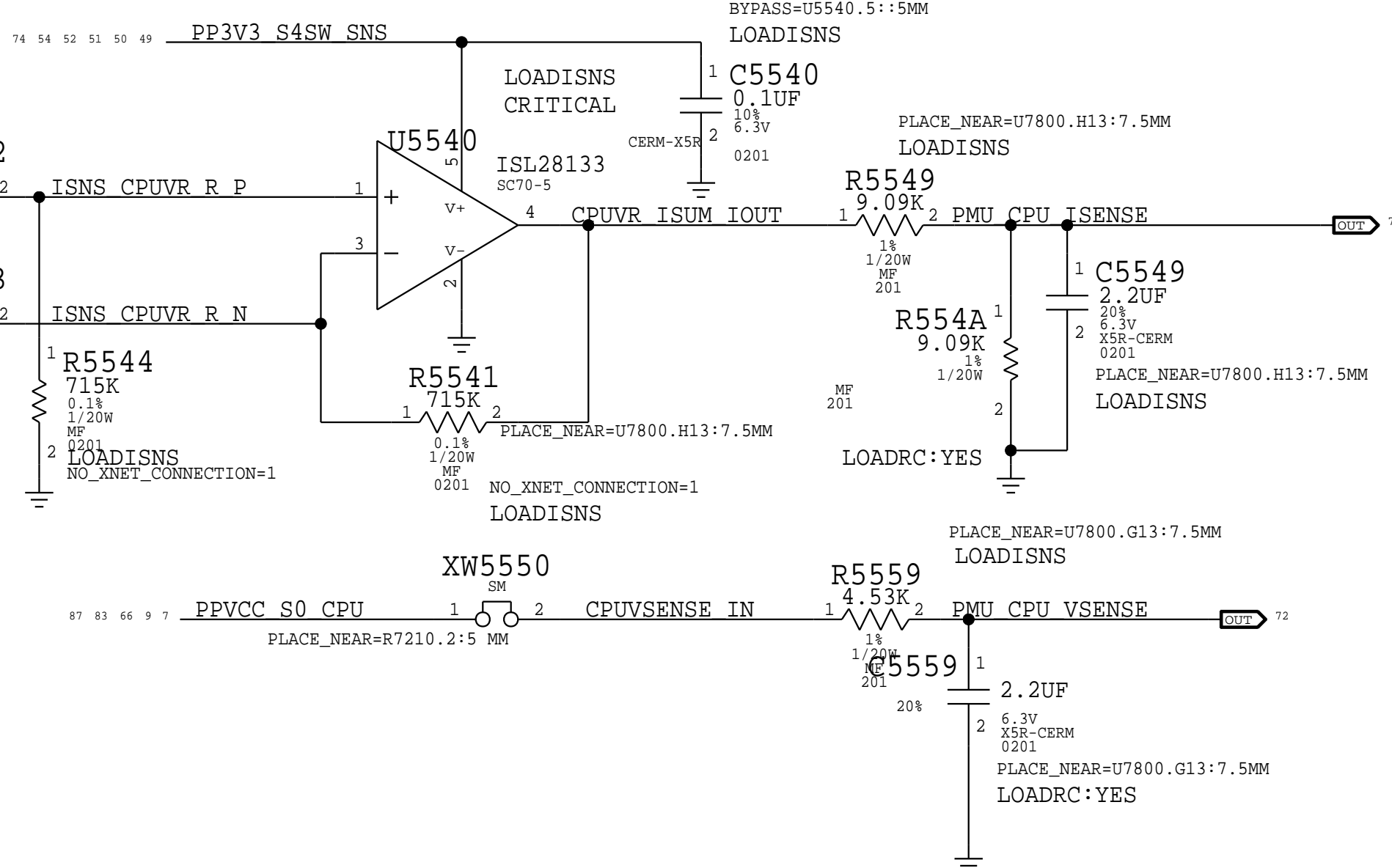
CPU Core Current Sense (ICAC)

Gain: 104.38x, EDP: 64 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 24 mV, Range: 76.64 A
PMU AMUX: B7



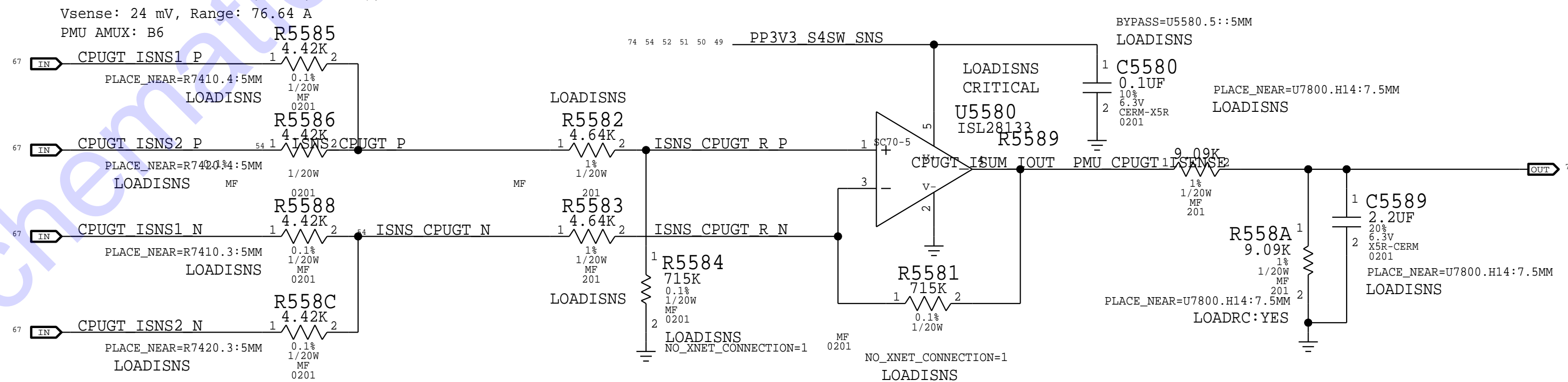
CPU Core Voltage Sense (VCAC)

PMU AMUX: B4



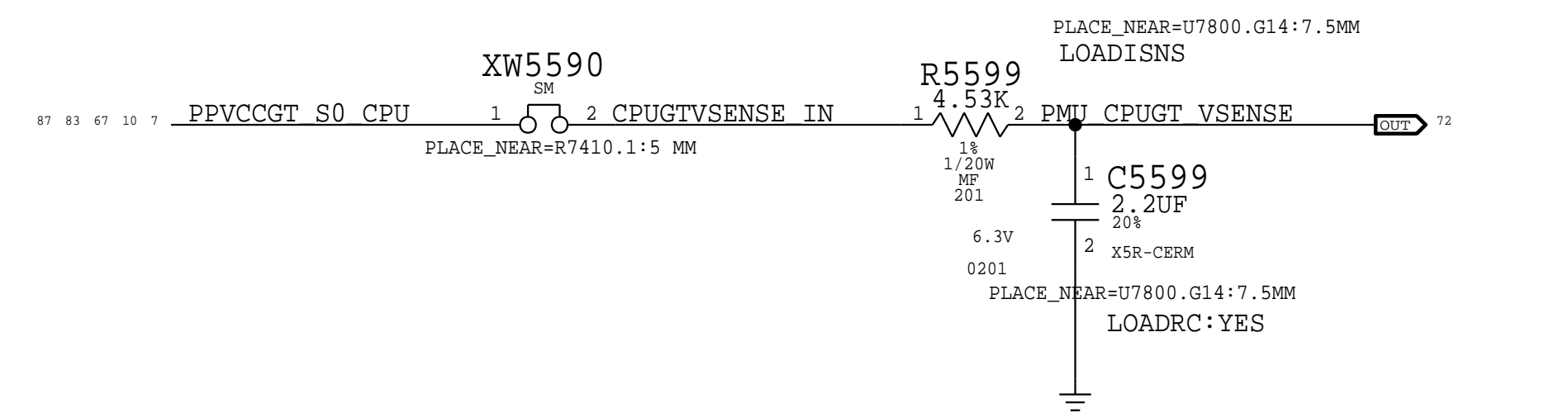
CPU GT+GTx Current Sense (ICGC)

Gain: 104.38x, EDP: 64 A
Rsense: 2x of 0.00075 (R7410, R7420), Rsum: 0.000375
Vsense: 24 mV, Range: 76.64 A
PMU AMUX: B6



CPU GT Voltage Sense (VCGC)

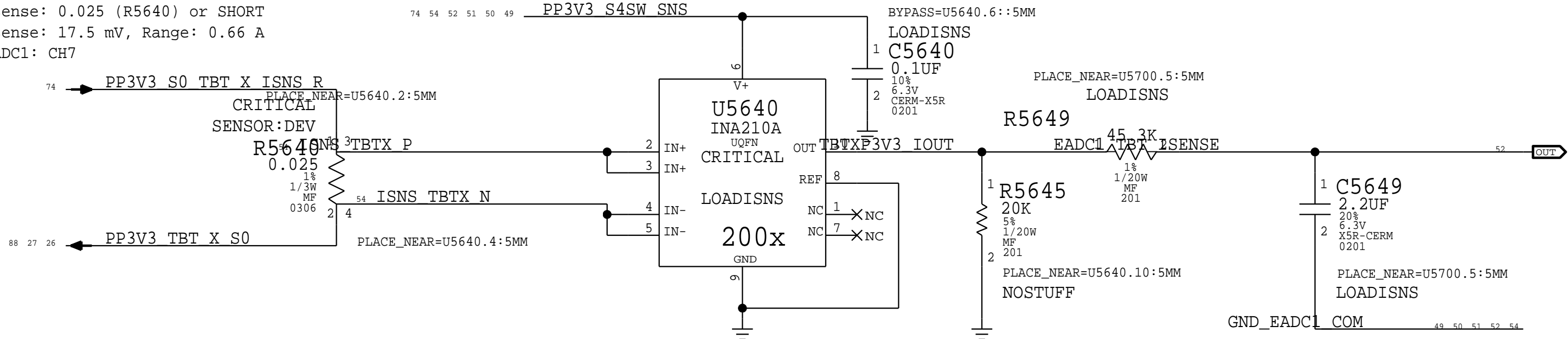
PMU AMUX: B5



PAGE TITLE		
POWER SENSORS LOAD SIDE		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
	BRANCH	evt-1
	PAGE	55 OF 500
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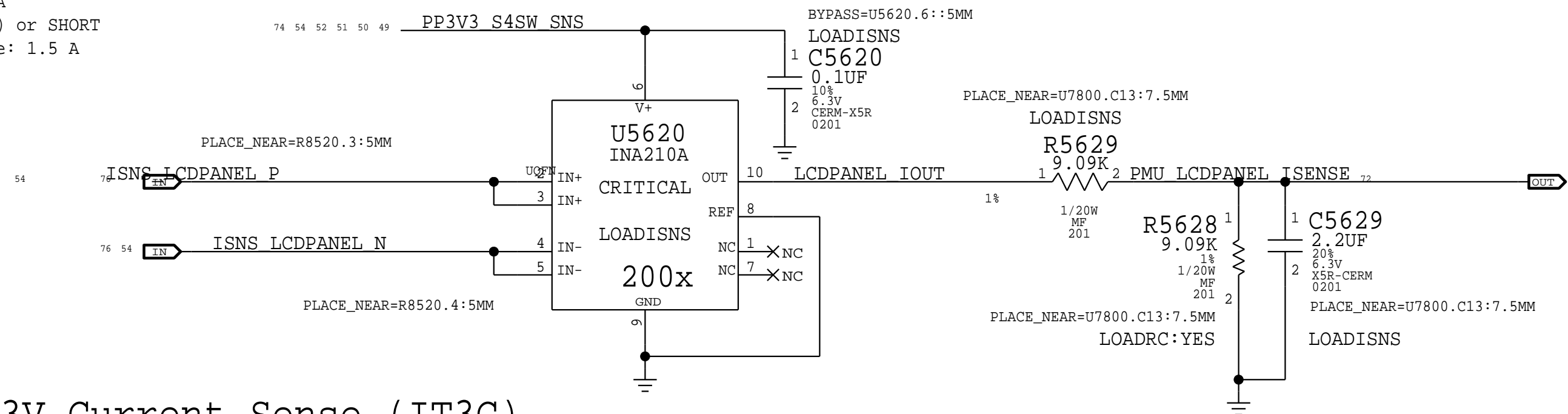
Thunderbolt TBD Left Current Sense (IULC)

Gain: 200x. EDP: 0.7 A
Rsense: 0.025 (R5640) or SHORT
Vsense: 17.5 mV, Range: 0.66 A
EADC1: CH7



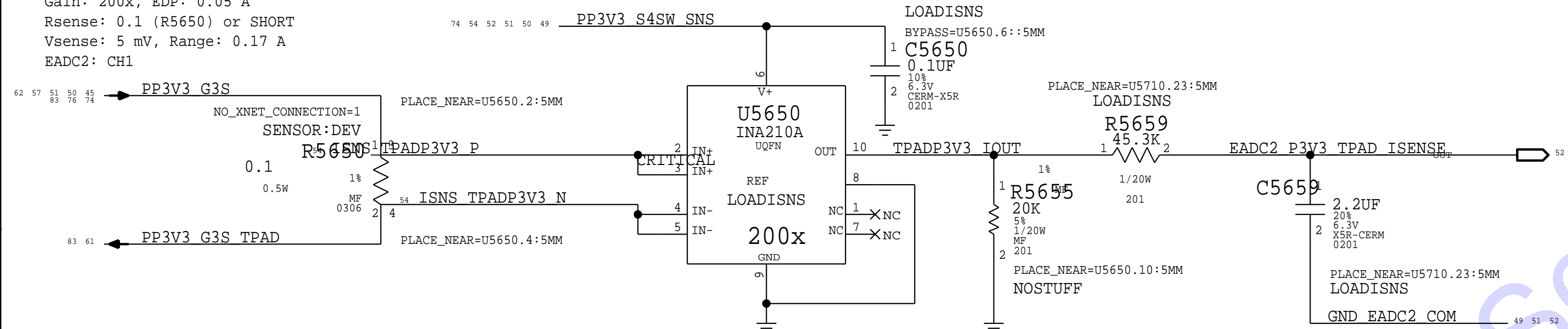
LCD Panel 3.3V Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R5620) or SHORT
Vsense: 10 mV, Range: 1.5 A
EADC2: CH0



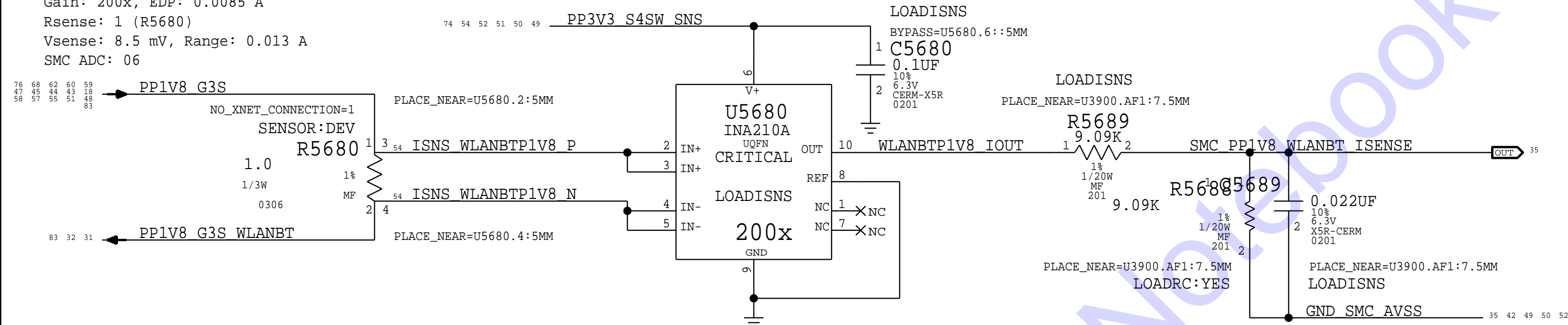
Trackpad 3V Current Sense (IT3C)

Gain: 200x. EDP: 0.05 A
Rsense: 0.1 (R5650) or SHORT
Vsense: 5 mV, Range: 0.17 A
EADC2: CH1



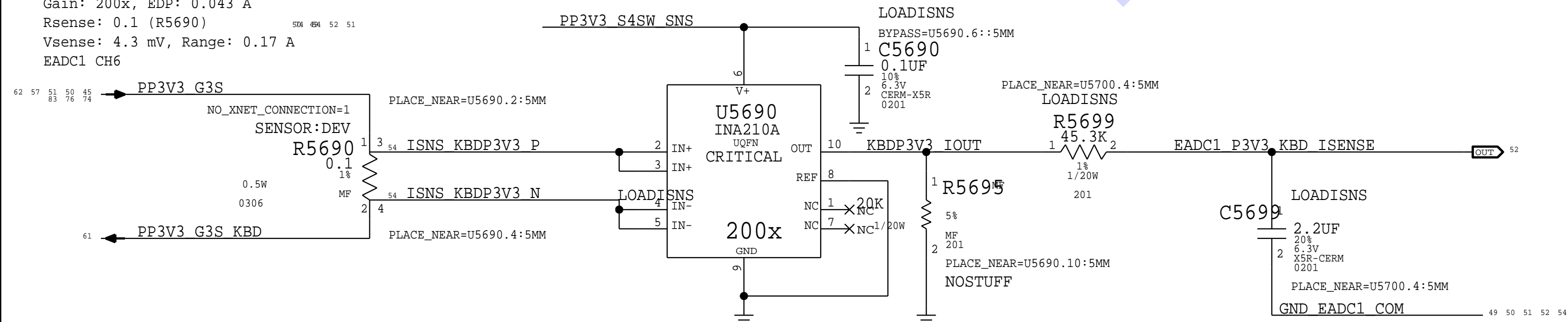
WLANBT 1.8V Current Sense (IW2C)

Gain: 200x. EDP: 0.0085 A
Rsense: 1 (R5680)
Vsense: 8.5 mV, Range: 0.013 A
SMC ADC: 06



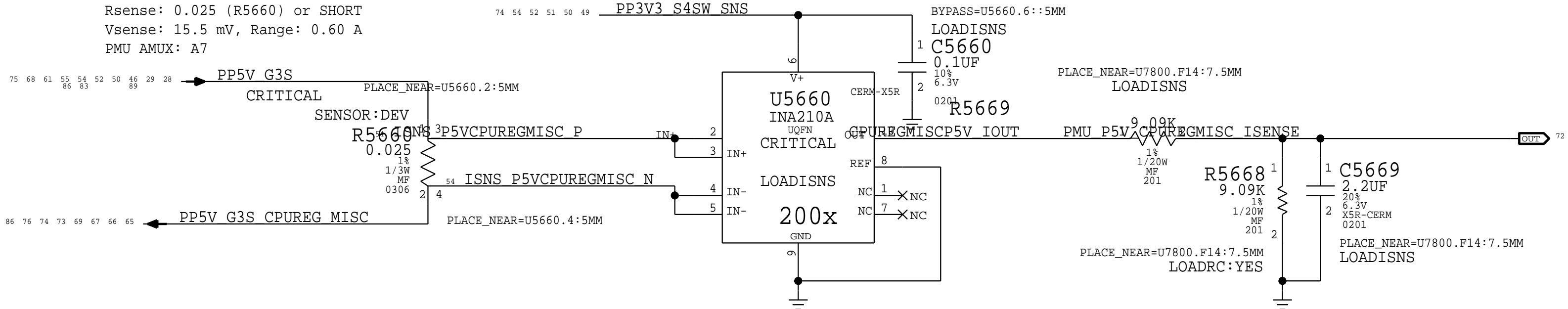
Keyboard 3.3V Current Sense (IK3C)

Gain: 200x. EDP: 0.043 A
Rsense: 0.1 (R5690)
Vsense: 4.3 mV, Range: 0.17 A
EADC1 CH6



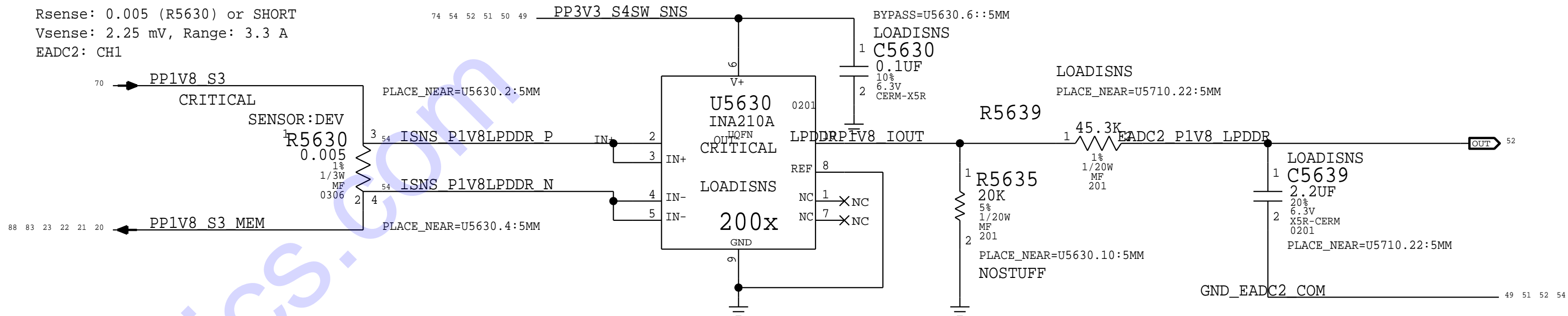
CPU Reg. ALSCAM, LCD 5V Current Sense (IC5C)

Gain: 200x. EDP: 0.42+0.1+0.1 A
Rsense: 0.025 (R5660) or SHORT
Vsense: 15.5 mV, Range: 0.60 A
PMU AMUX: A7



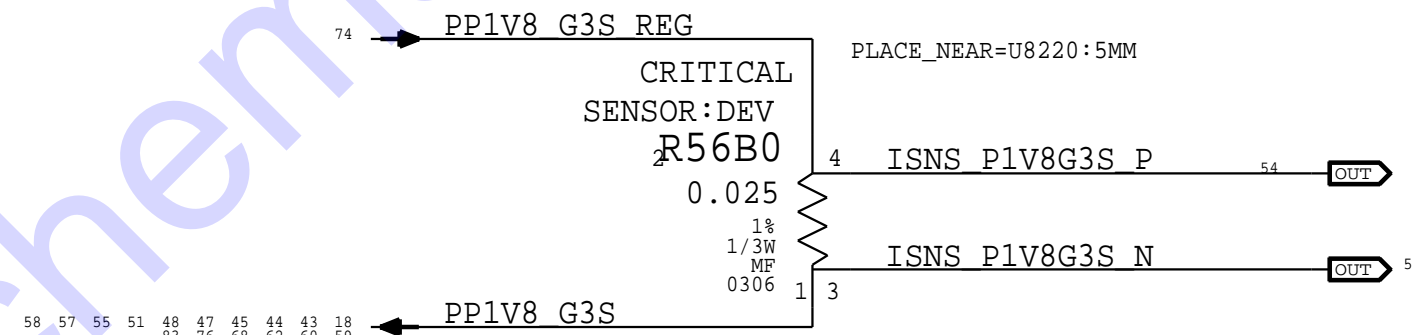
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x. EDP: 0.45 A
Rsense: 0.005 (R5630) or SHORT
Vsense: 2.25 mV, Range: 3.3 A
EADC2: CH1

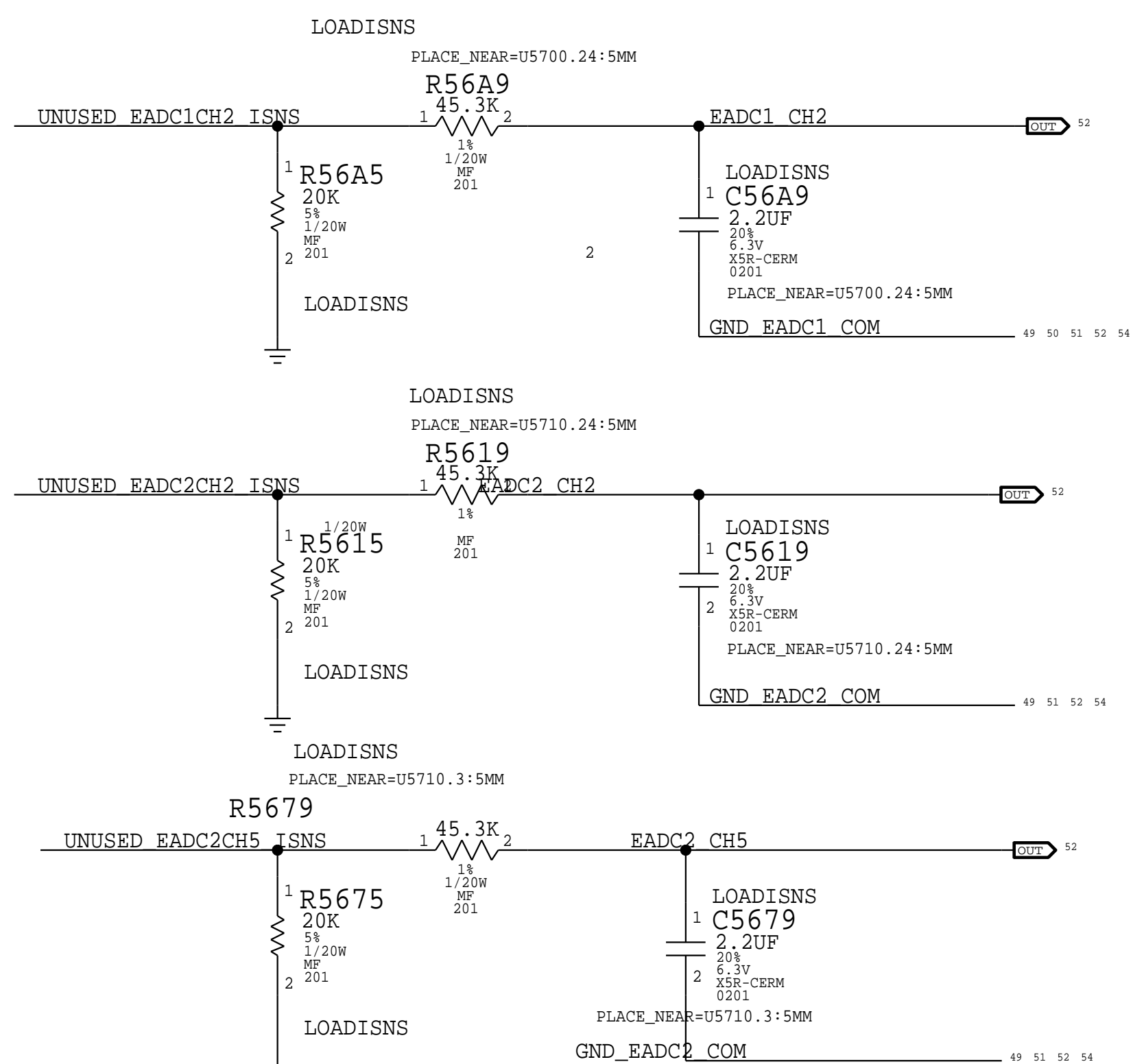


1.8V Standby Current Sense

Gain: None. EDP: 0.65 A
Rsense: 0.025 (R56B0) or SHORT
Vsense: 16.25 mV



UNUSED ADC CHANNELS



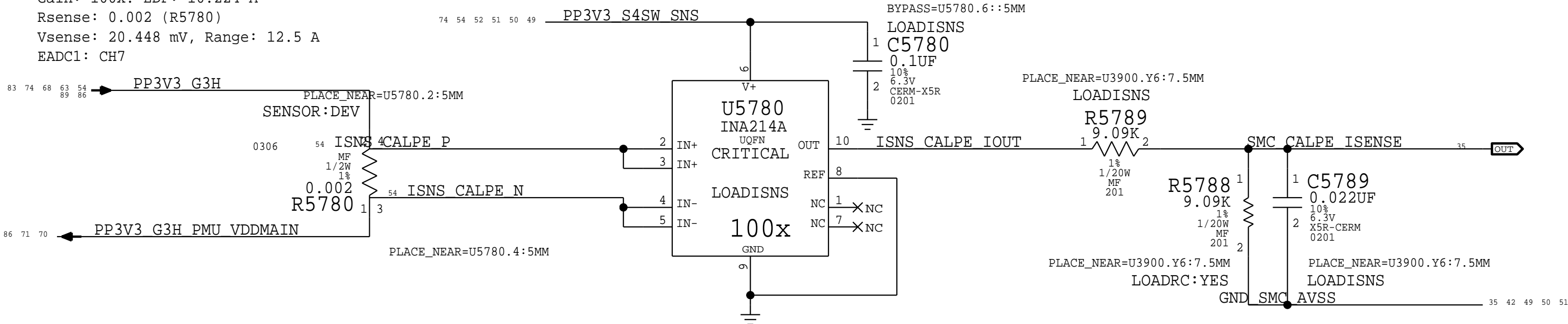
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	R5628, R5688	R5628, R5688	CRITICAL	LOADRC:NO

BOM_COST_GROUP=SENSORS

POWER SENSORS EXTENDED		
	DRAWING NUMBER	051-04273
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	PAGE	56 OF 500
	SHEET	51 OF 98

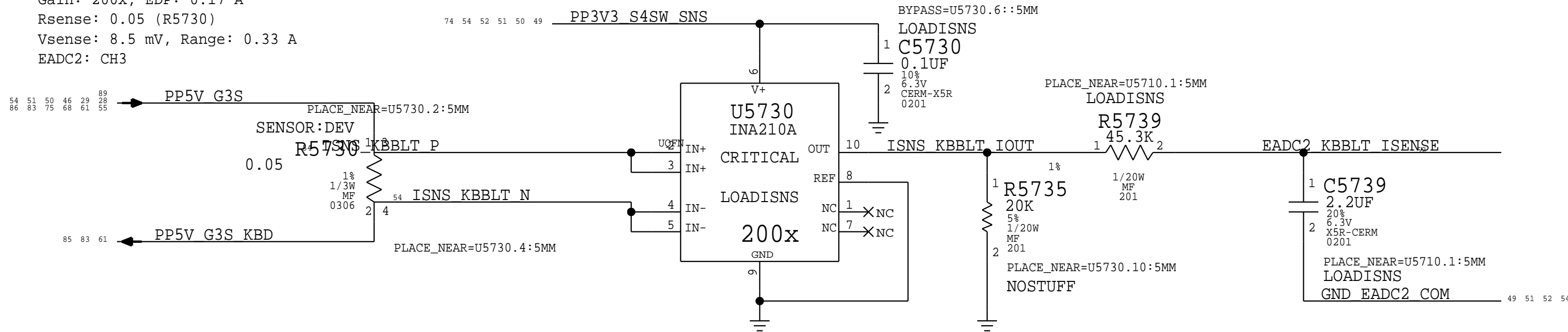
Calpe 3.3V Input Current Left (IP3C)

Gain: 100x, EDP: 10.224 A
Rsense: 0.002 (R5780)
Vsense: 20.448 mV, Range: 12.5 A
EADC1: CH7



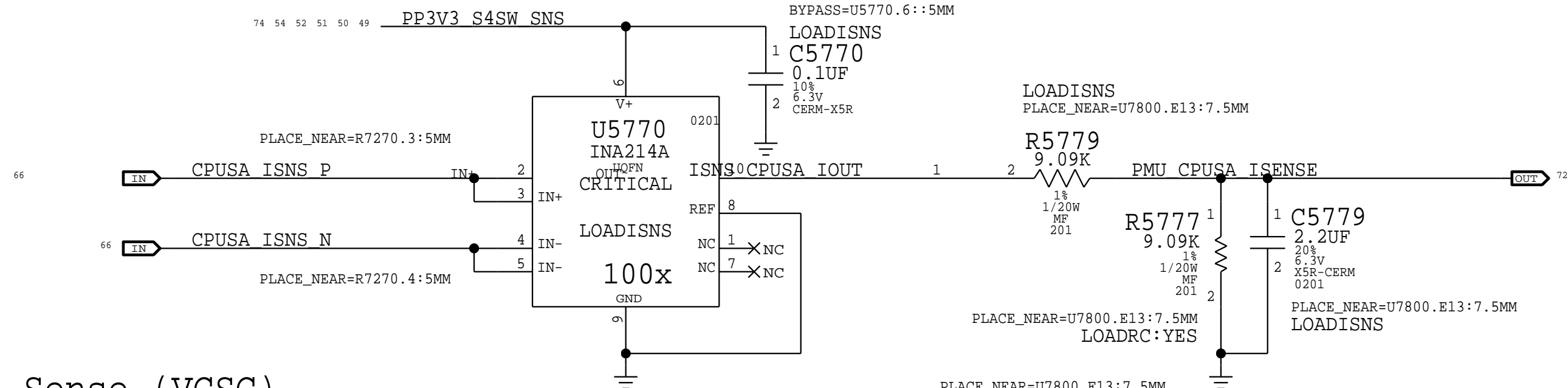
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 0.17 A
Rsense: 0.05 (R5730)
Vsense: 8.5 mV, Range: 0.33 A
EADC2: CH3



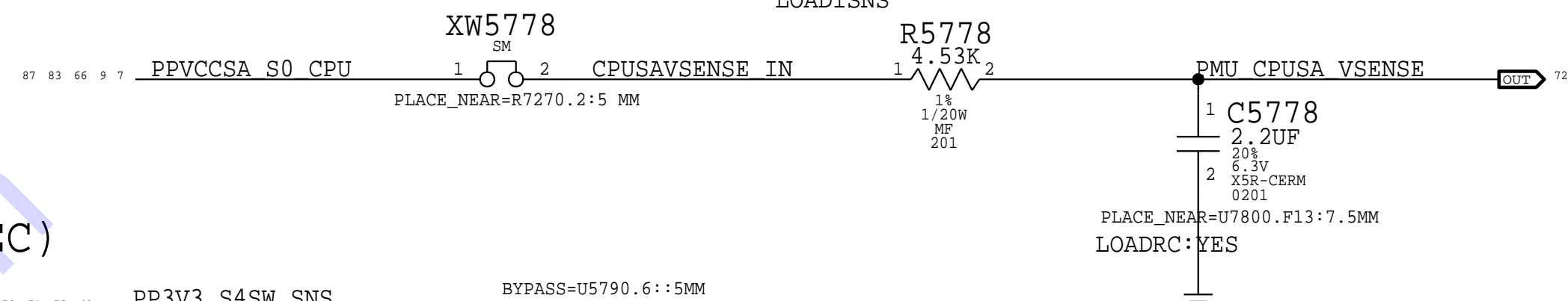
CPU SA Current Sense (ICSC)

Gain: 100X, EDP: 9.5 A
Rsense: 0.002 (R7270)
Vsense: 19 mV, Range: 15 A
PMU AMUX: B1



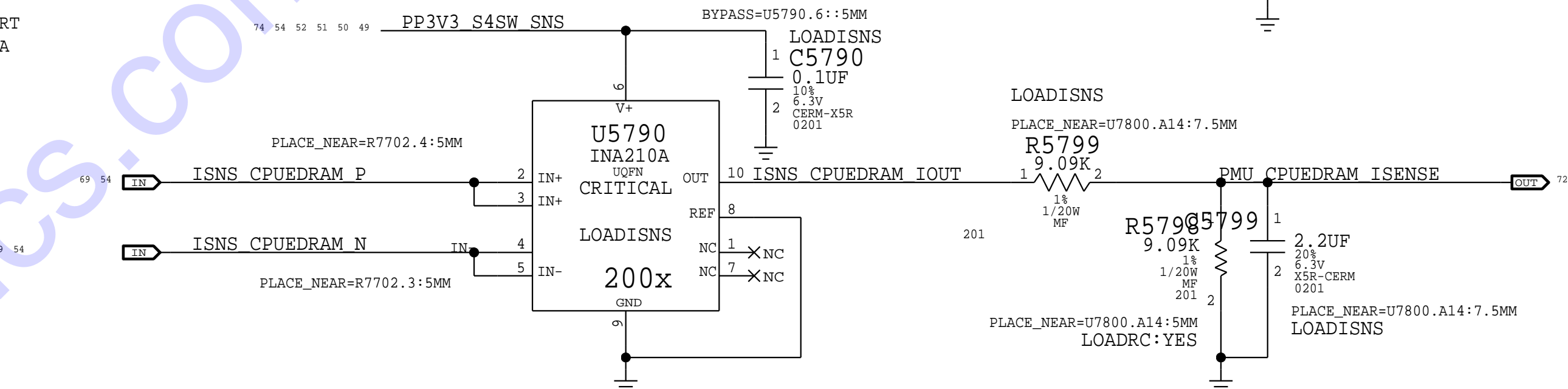
CPU SA Voltage Sense (VCSC)

PMU AMUX: B3



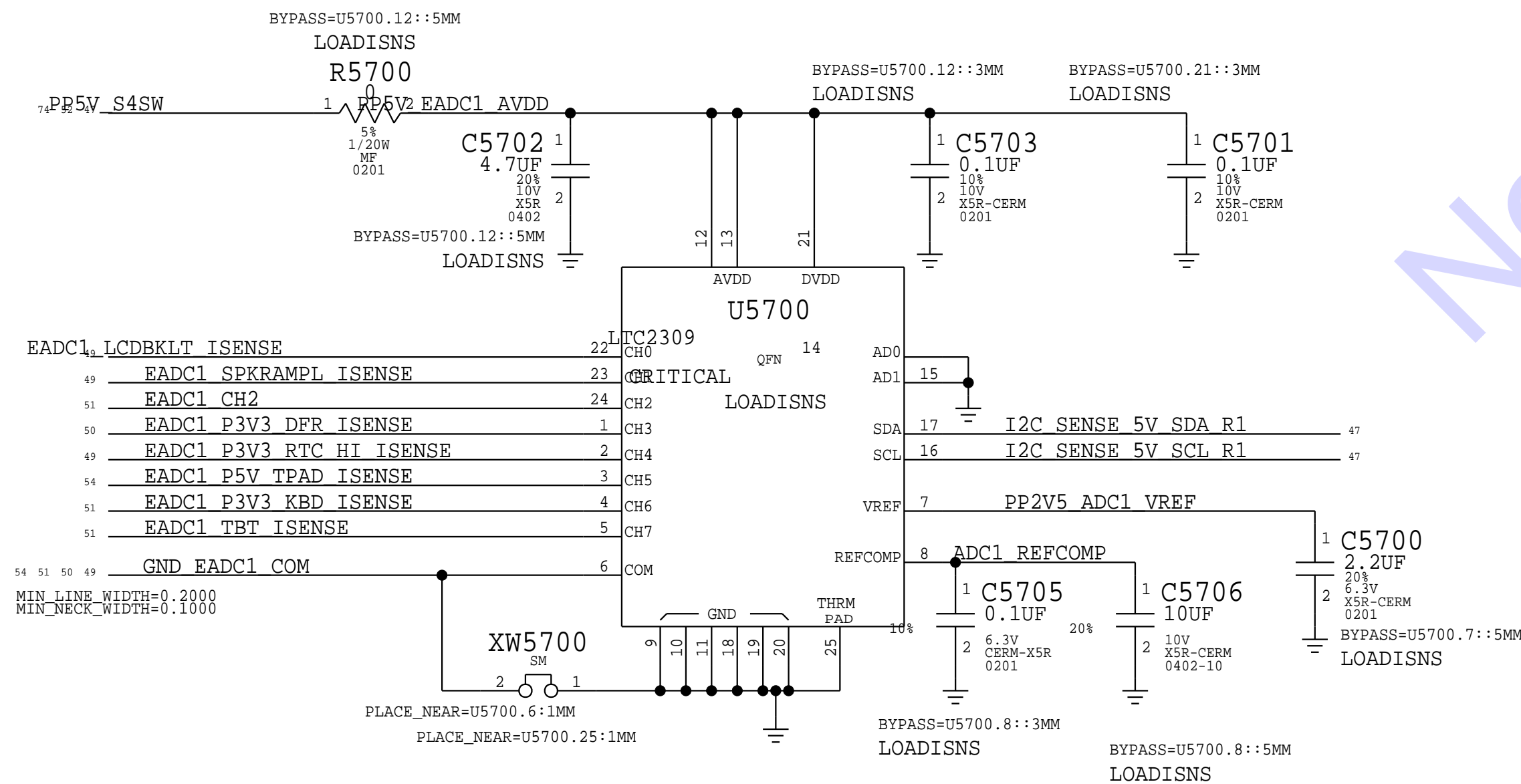
CPU EDRAM Current Sense (ICEC)

Gain: 200x, EDP: 6.2 A
Rsense: 0.002 (R7702) or SHORT
Vsense: 12.4 mV, Range: 7.5 A
PMU AMUX: A2



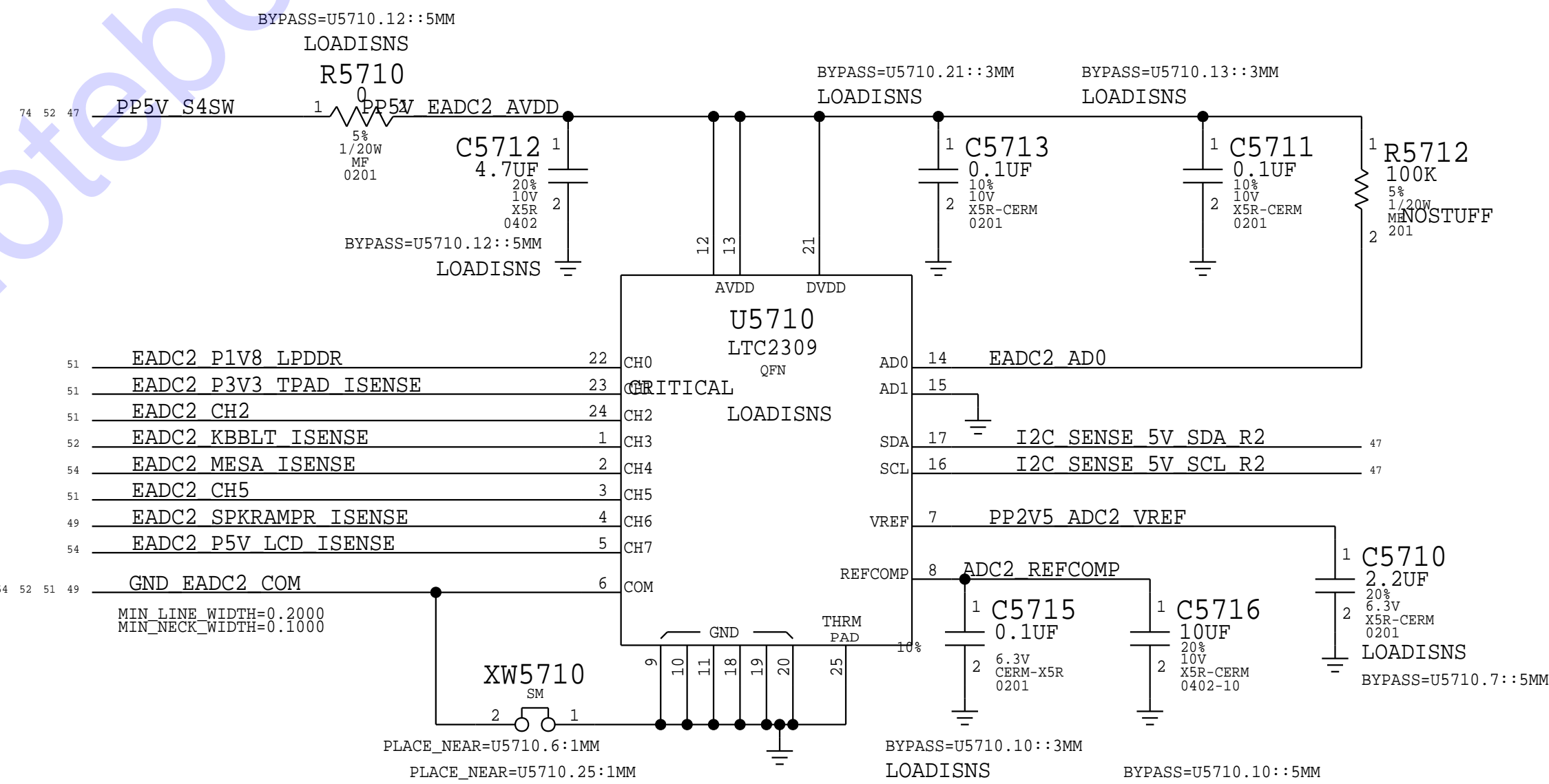
EADC1

(Write: 0x10 Read: 0x11)



EADC2

(Write: 0x12 Read: 0x13)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	R5768,R5777,R5788,R5798,C5778		LOADRC:NO

POWER SENSORS EXTENDED 2		
	DRAWING NUMBER	051-04273
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	PAGE	57 OF 500
	SHEET	52 OF 98

BOM_COST_GROUP=SENSORS

Thermal Sensor A:
TBT Die, NAND, WIFI, I/O proximity

I2C Write: 0x90, I2C Read: 0x91

TBT Die Thermal Diode (TBA)

Placement Note:
The P leg connects to THERMDA of TBT die.
The N leg connectd to GND pin close to THERMDA.

WIFI Proximity (TW0P)

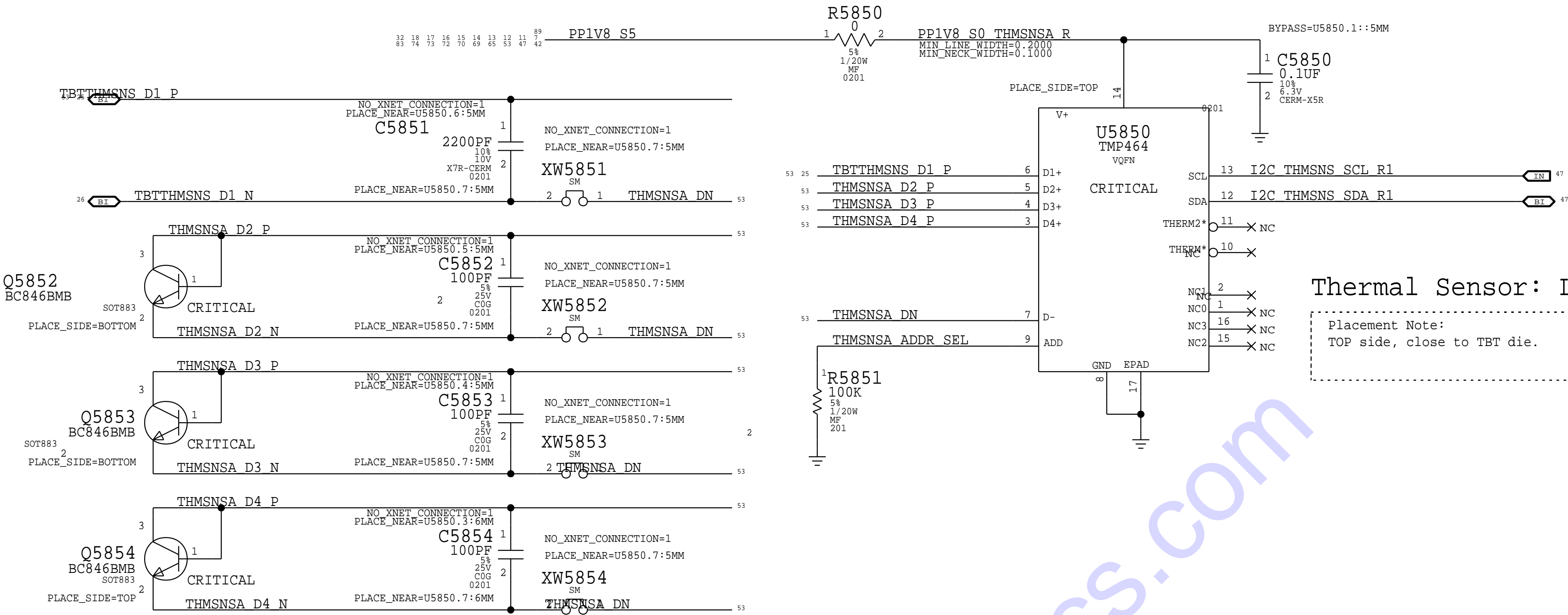
Placement Note:
BOTTOM side of WIFI/BT module

NAND Proximity #1 (TH0b)

Placement note:
BOTTOM side between NAND devices

NAND Proximity #2 (TH0a)

Placement note:
TOP side between NAND devices



Thermal Sensor B
Fin Stack, CPU Proximity, Memory Proximity, and CPU VR

I2C Write: 0x92, I2C Read: 0x93

Thermal Diode: Ambient (TA0p)

Placement Note:
Airflow thermal indicator, TOP side.

CPU Proximity (TC0P)

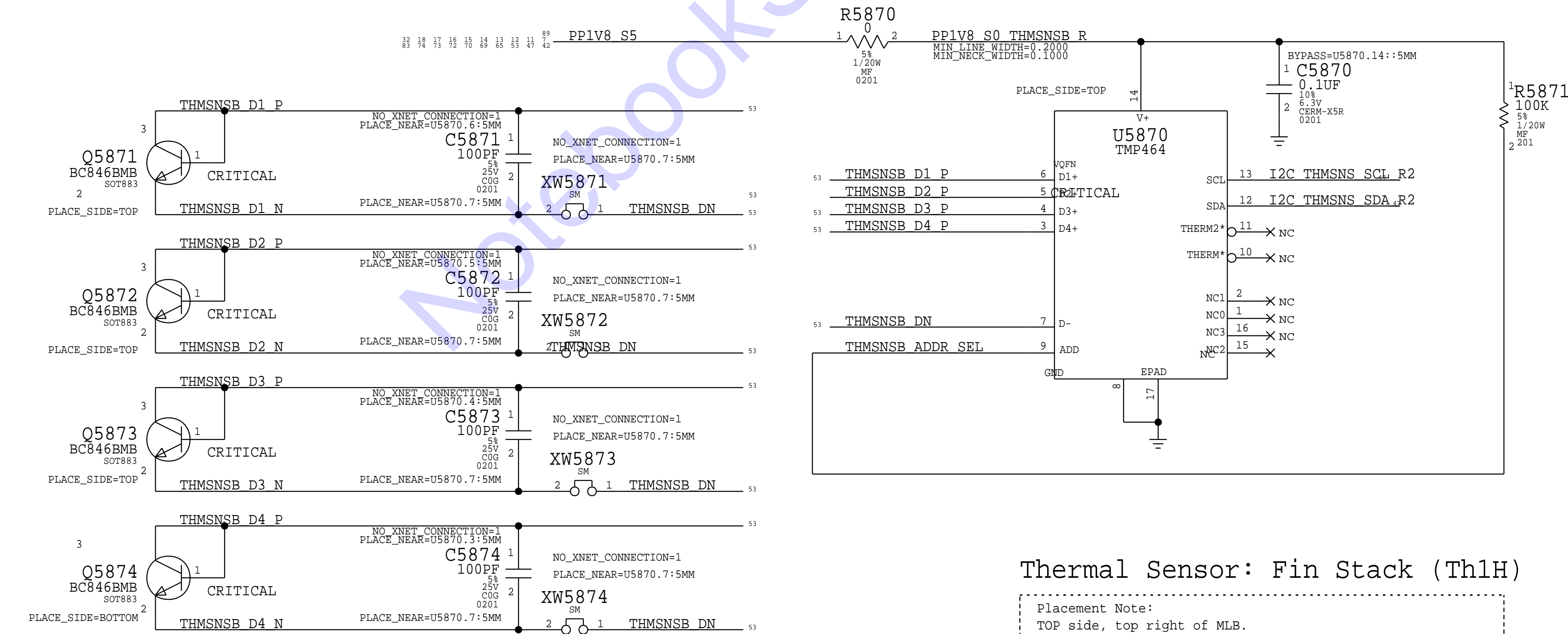
Placement Note:
TOP side of CPU.

Memory Proximity (TM0P)

Placement Note:
TOP side between main memory devices.

Memory Proximity (TM1P)

Placement Note:
BOTTOM side between main memory devices.

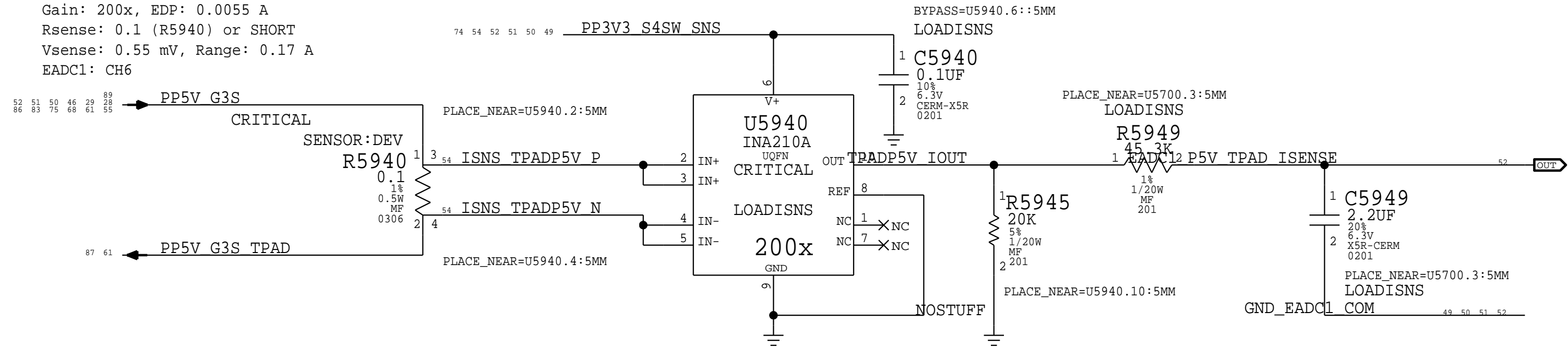


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THERMAL SENSORS		
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	PAGE	58 OF 500
	SHEET	53 OF 98

BOM_COST_GROUP=SENSORS

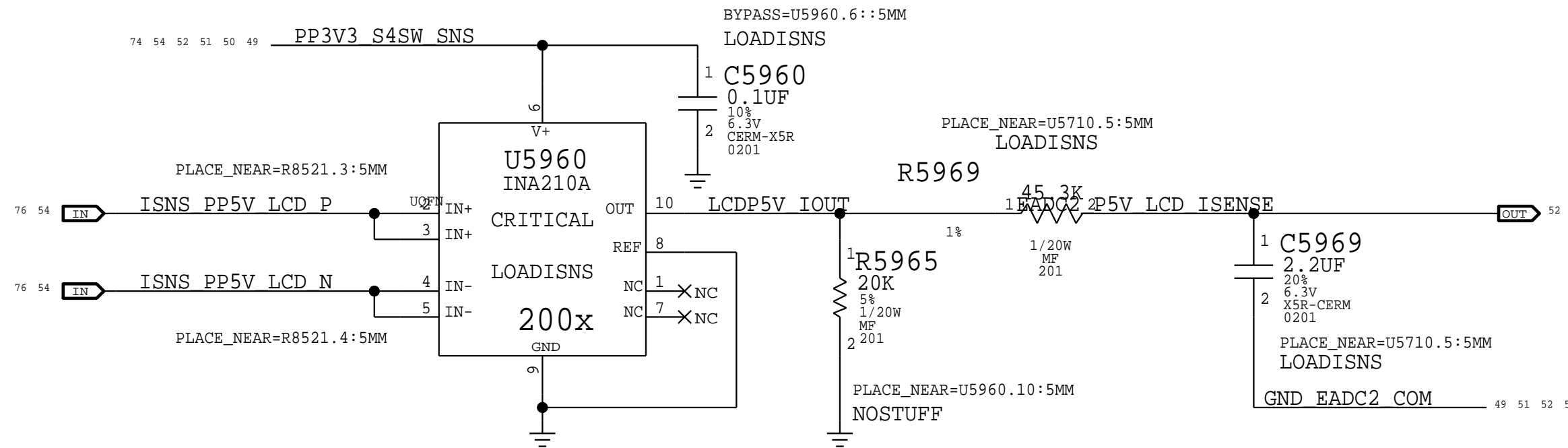
Trackpad 5V Current Sense (IT5C)

Gain: 200x, EDP: 0.0055 A
Rsense: 0.1 (R5940) or SHORT
Vsense: 0.55 mV, Range: 0.17 A
EADC1: CH6



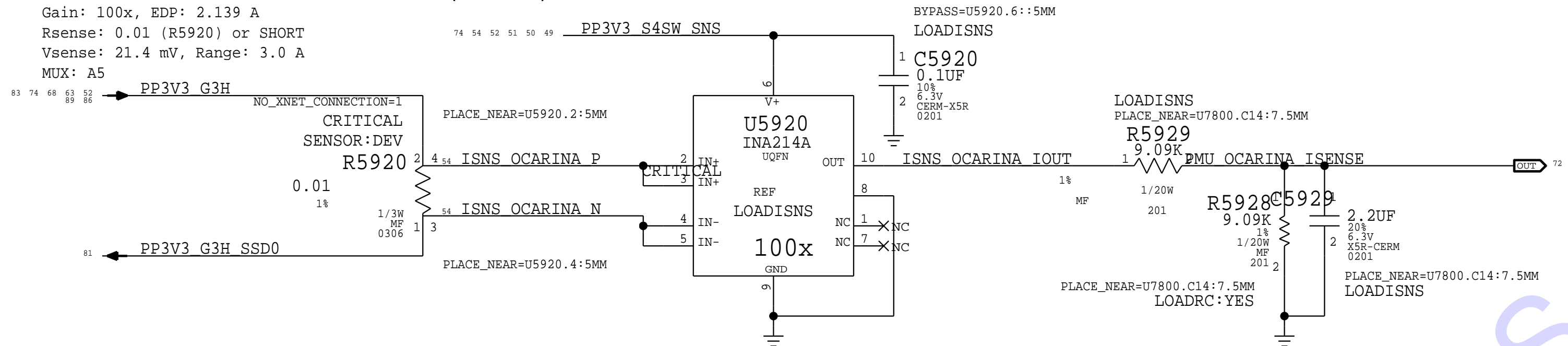
LCD Panel 5V Current Sense (IL5C)

Gain: 200x, EDP: 0.1 A
Rsense: 0.1 (R5921) or SHORT
Vsense: 10 mV, Range: 0.17 A
EADC1: CH7



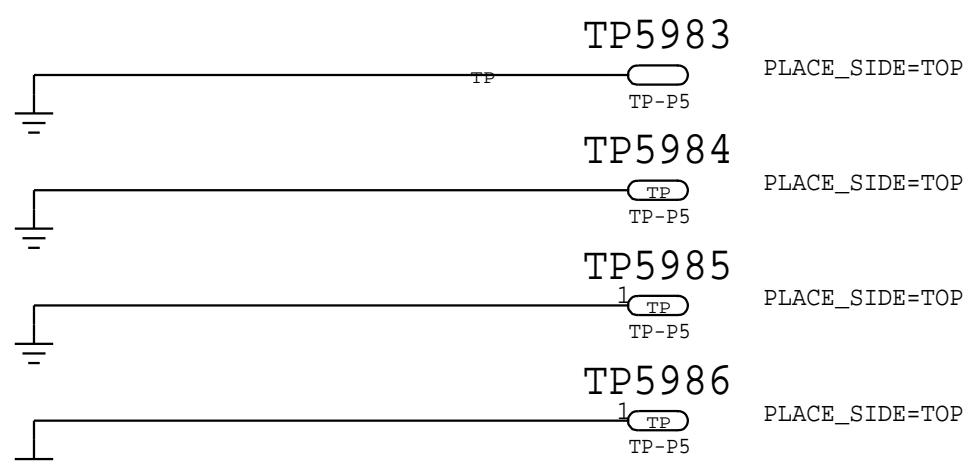
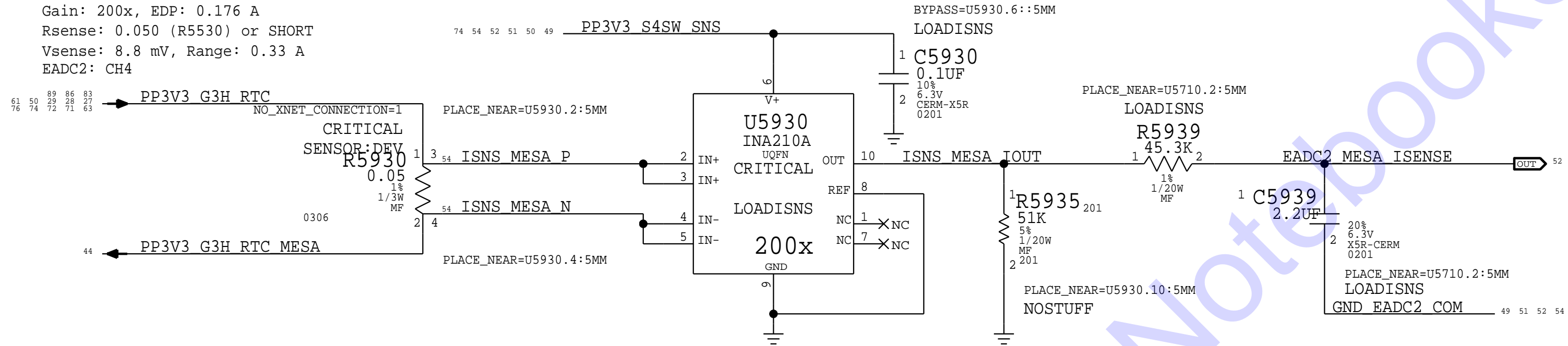
Ocarina Current Sense (IHCC)

Gain: 100x, EDP: 2.139 A
Rsense: 0.01 (R5920) or SHORT
Vsense: 21.4 mV, Range: 3.0 A
MUX: A5

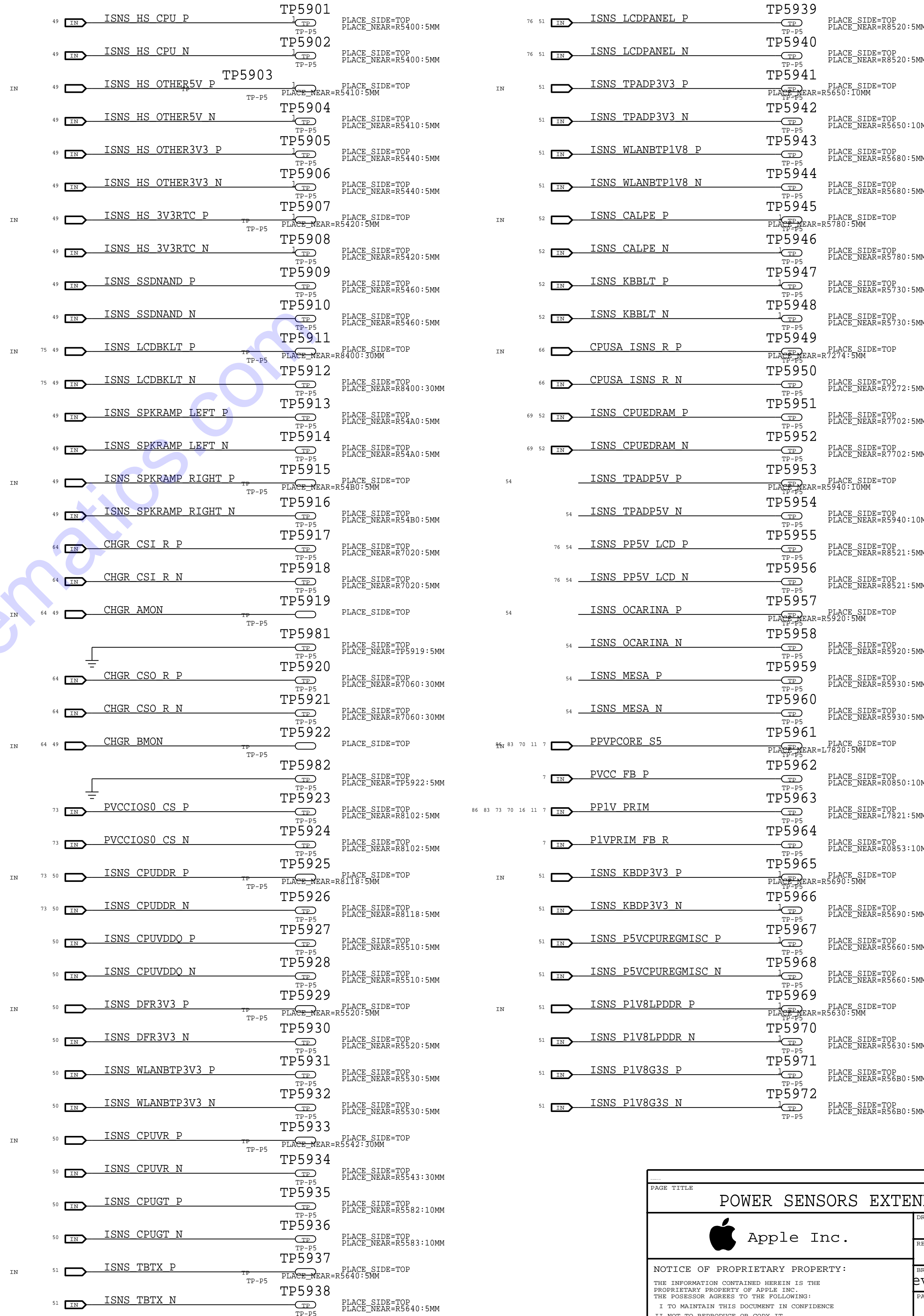


MESA Current Sense (IIDC)

Gain: 200x, EDP: 0.176 A
Rsense: 0.050 (R5930) or SHORT
Vsense: 8.8 mV, Range: 0.33 A
EADC2: CH4



Probe Points for Power Validation

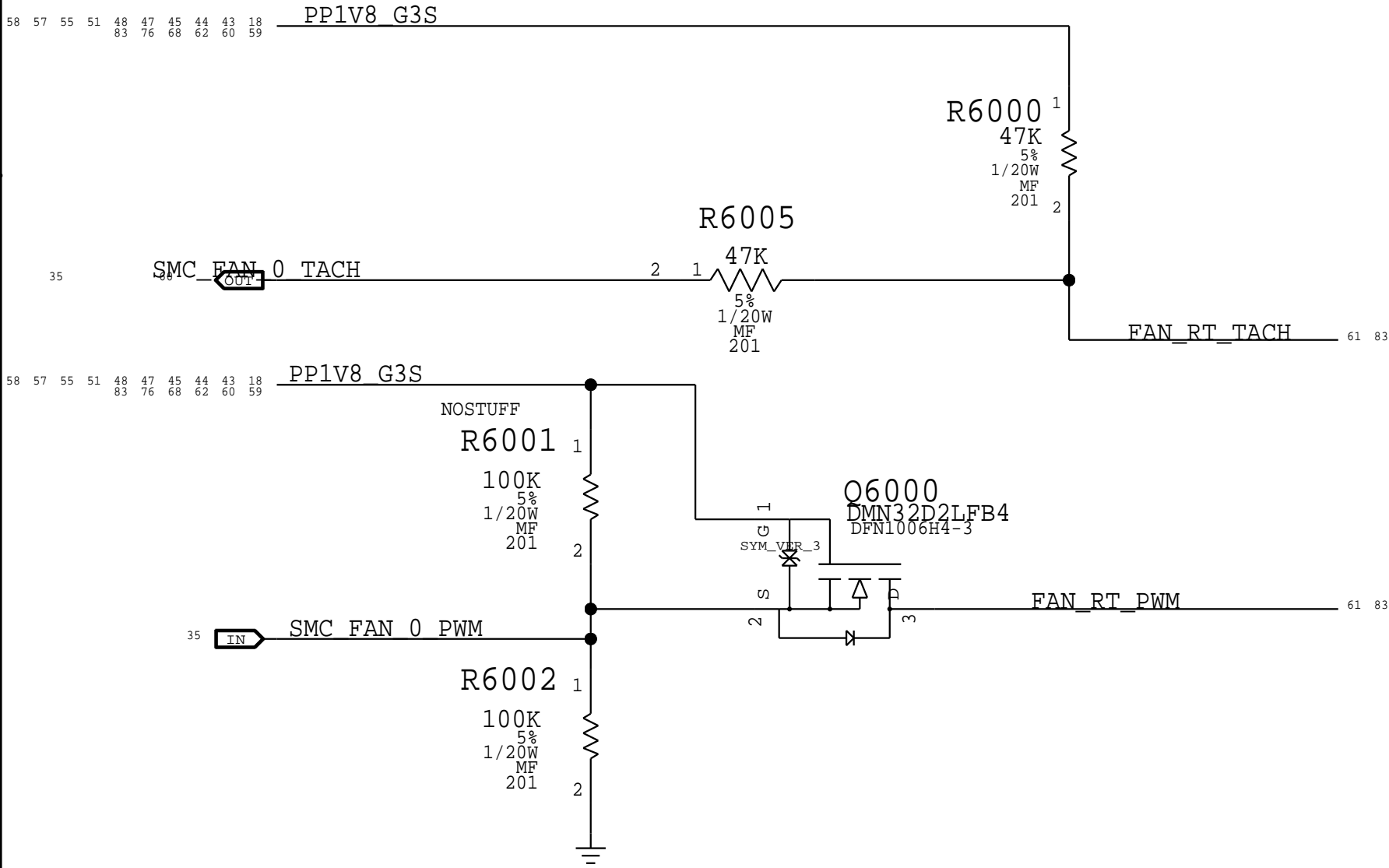


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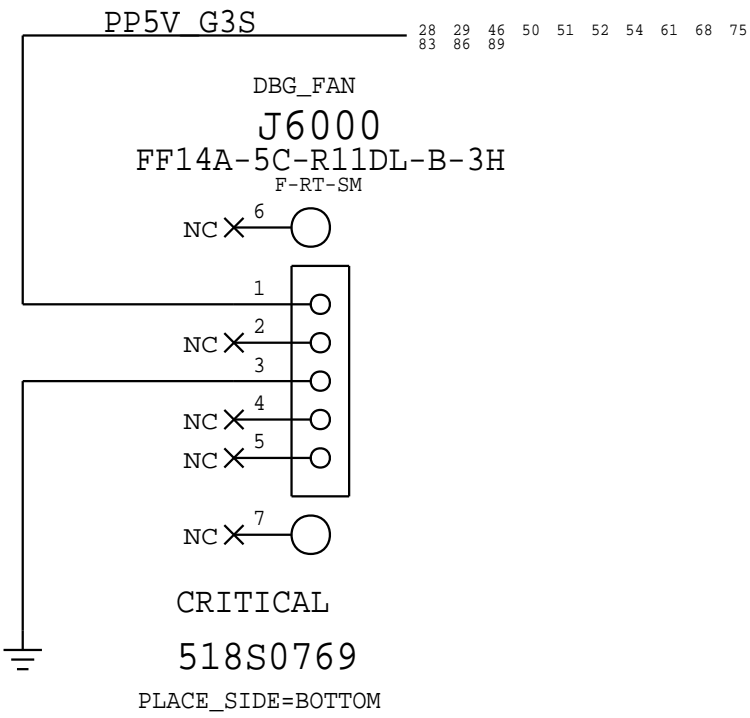
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	PAGE	59 OF 500
	SHEET	54 OF 98

FAN CONTROL



FOR DEBUG FAN POWER



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FANS/SMC/AMUX SUPPORT			
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		SHEET	55 OF 98

BOM_COST_GROUP=FAN

8		7		6		5		4		3		2		1	
D														D	
														C	
														B	
A														A	
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SYNC_DATE=05/29/2018

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BRANCH

evt-1

PAGE

62 OF 500

SHEET

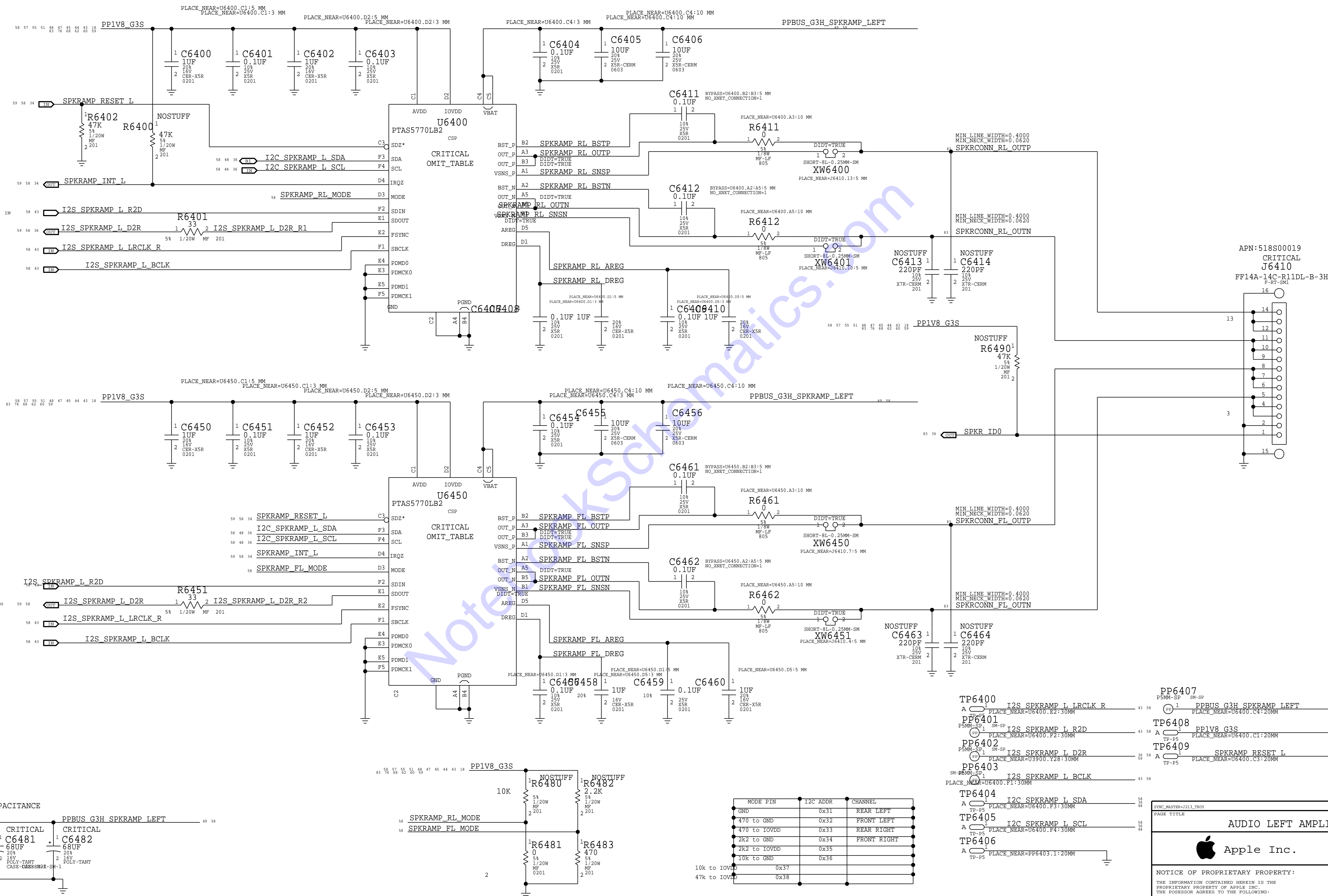
56 OF 98

SIZE

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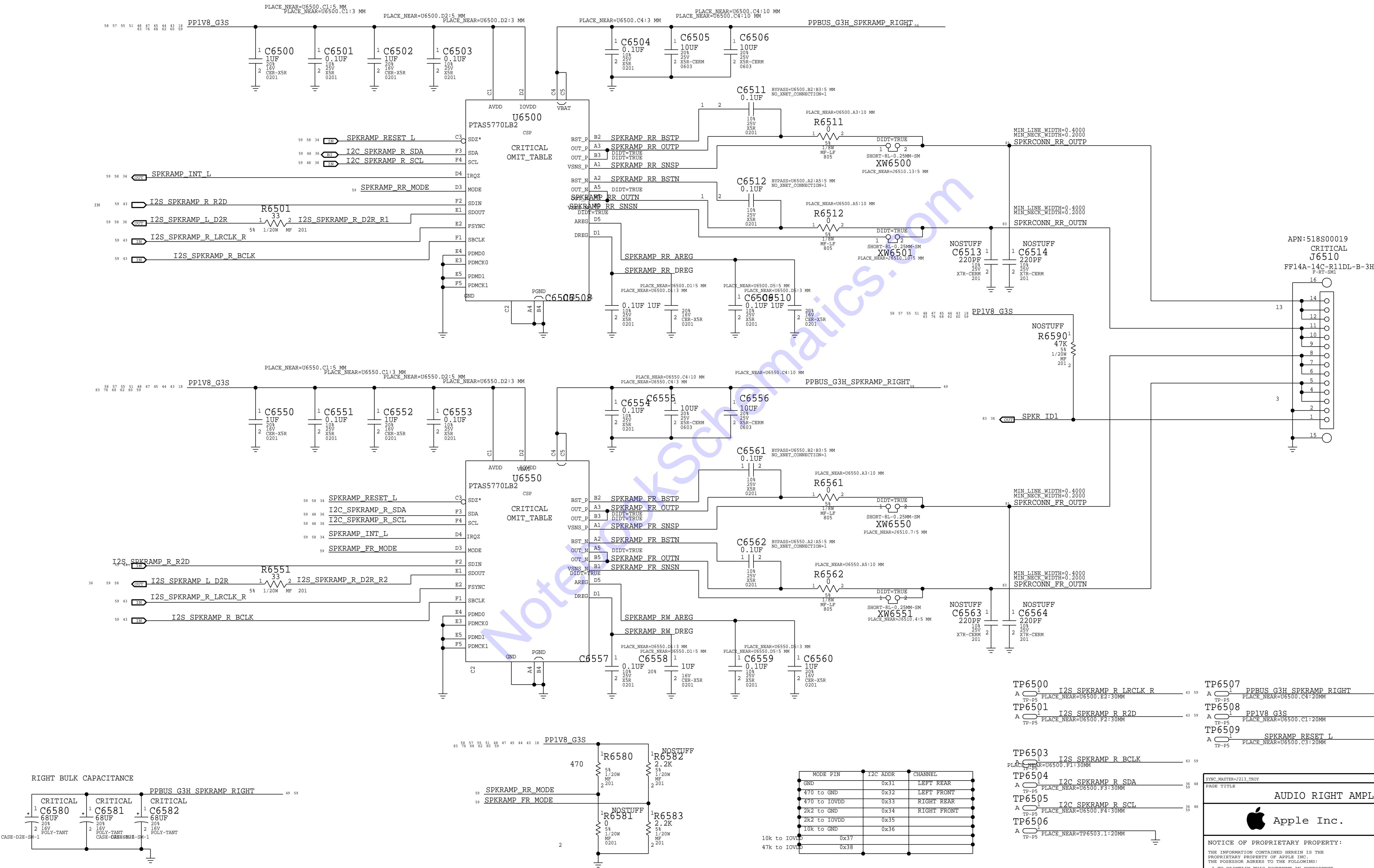
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2X MONO SPEAKER LEFT AMPLIFIERS


APN: 353S01252
GAIN: 0DBFS = xxVRMS

BOM_COST_GROUP=AUDIO

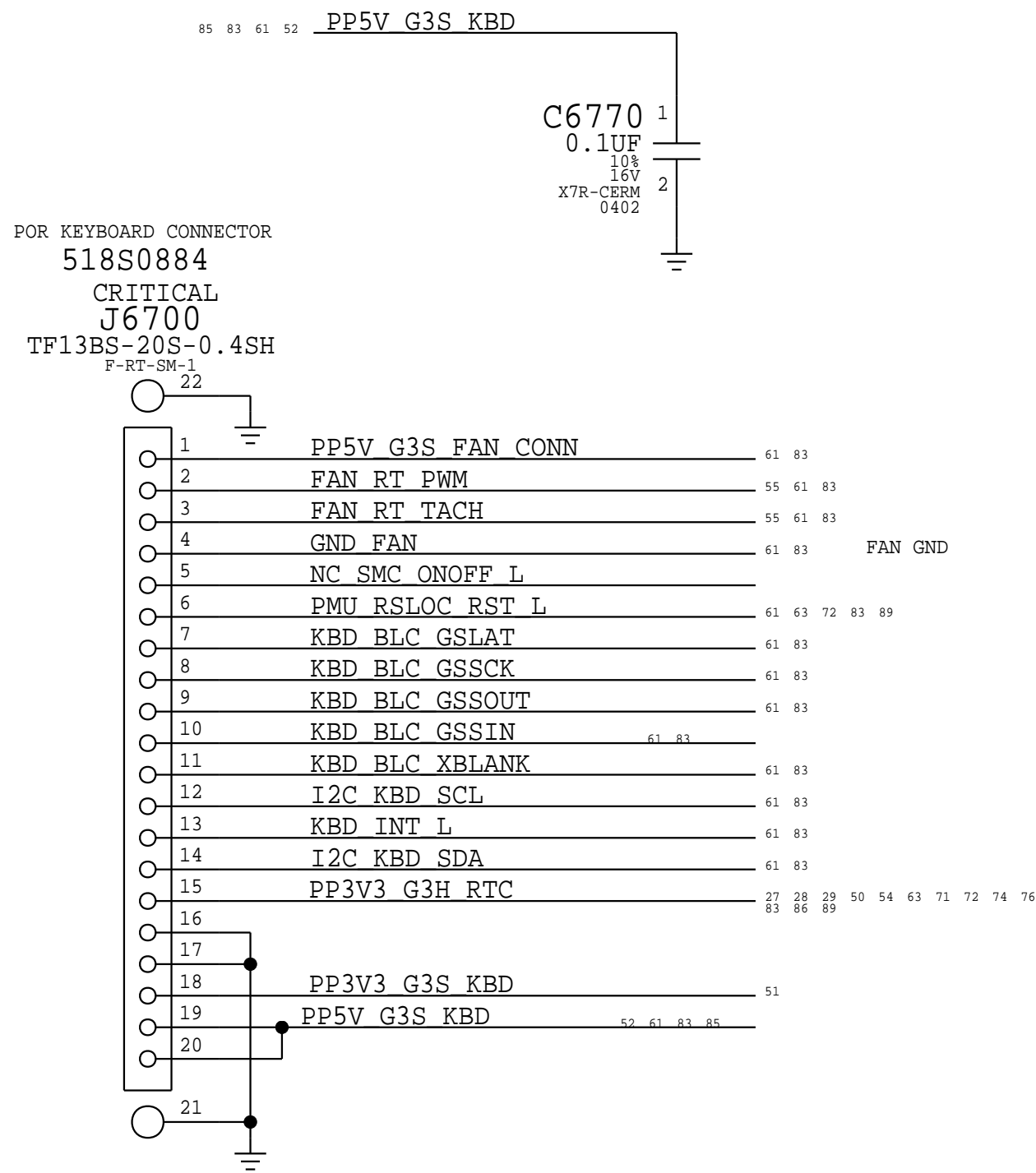
2X MONO SPEAKER RIGHT AMPLIFIERS

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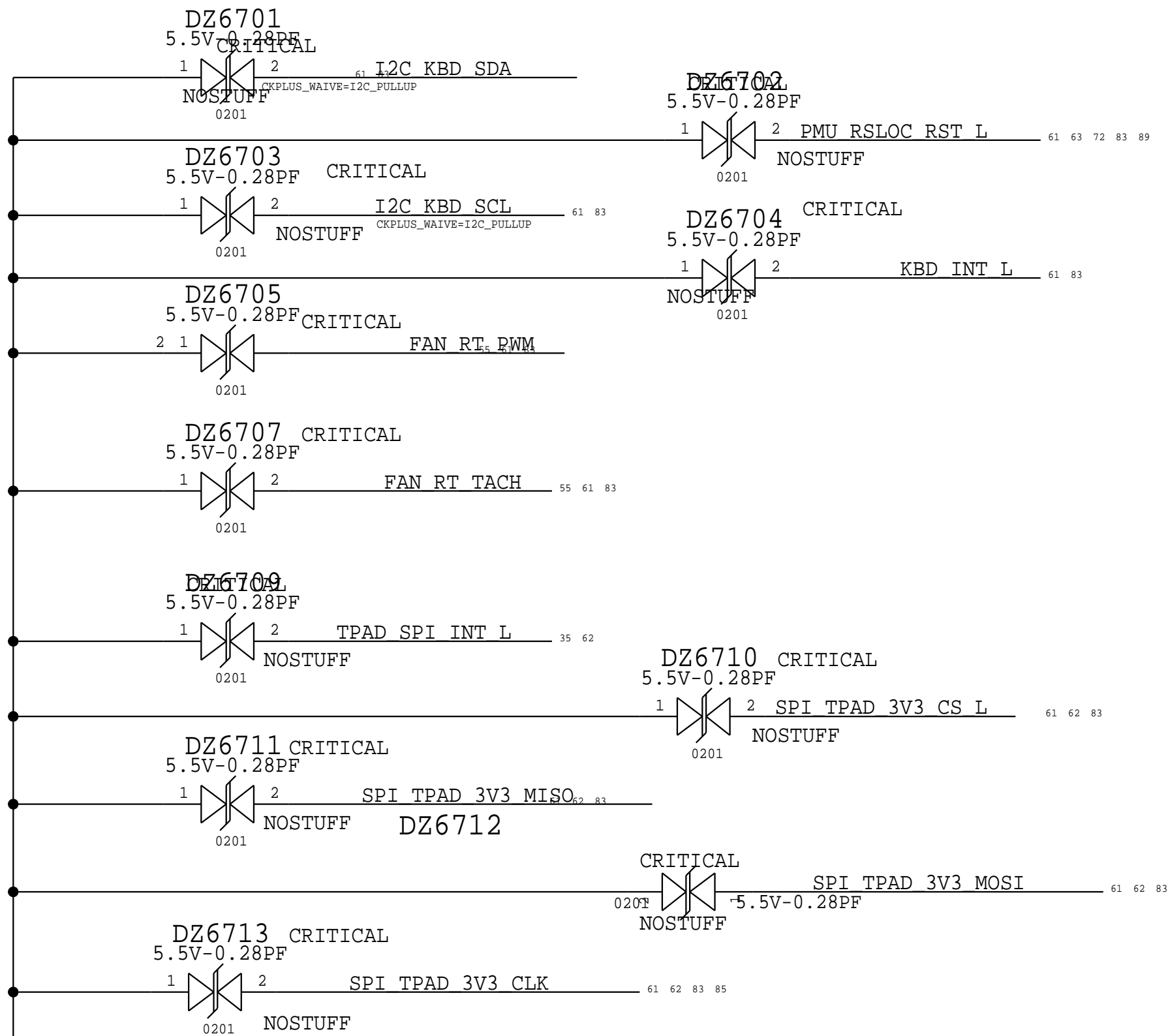
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		PAGE	65 OF 500
		SHEET	59 OF 98

KEYBOARD CONNECTOR

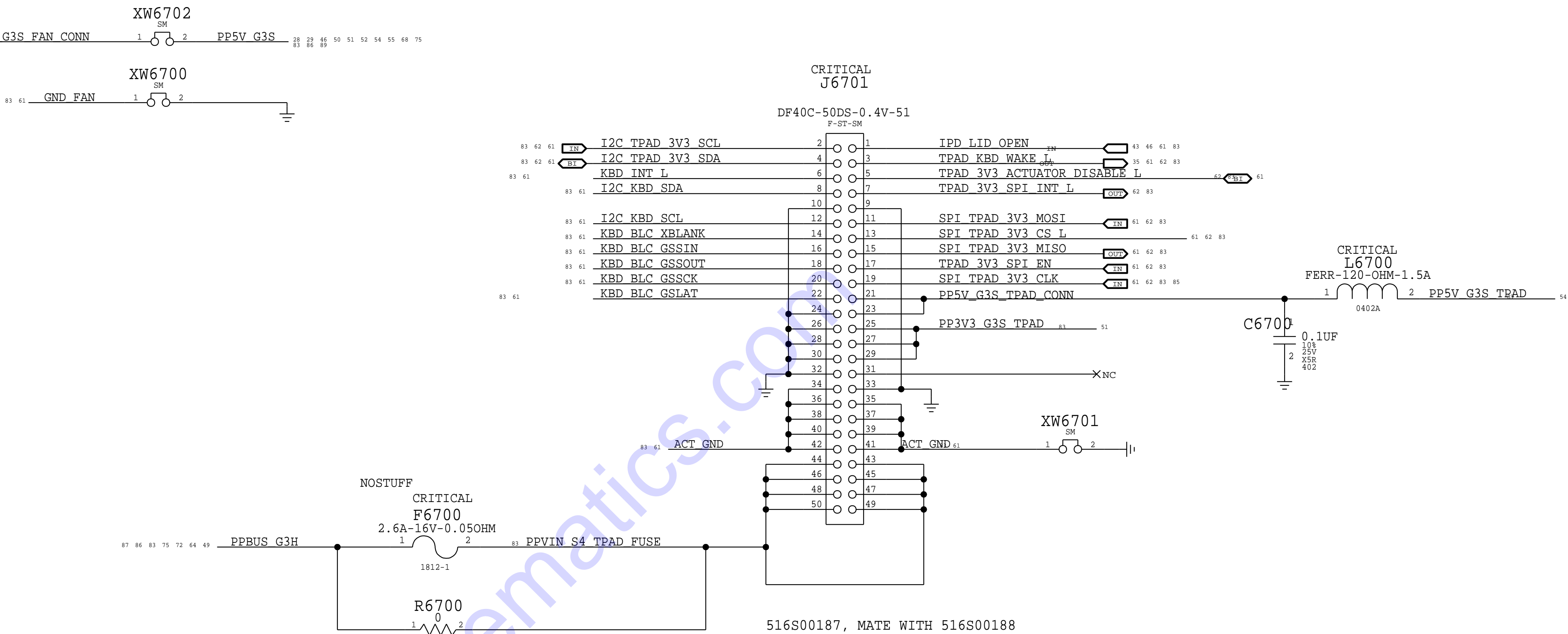


ESD DIODES

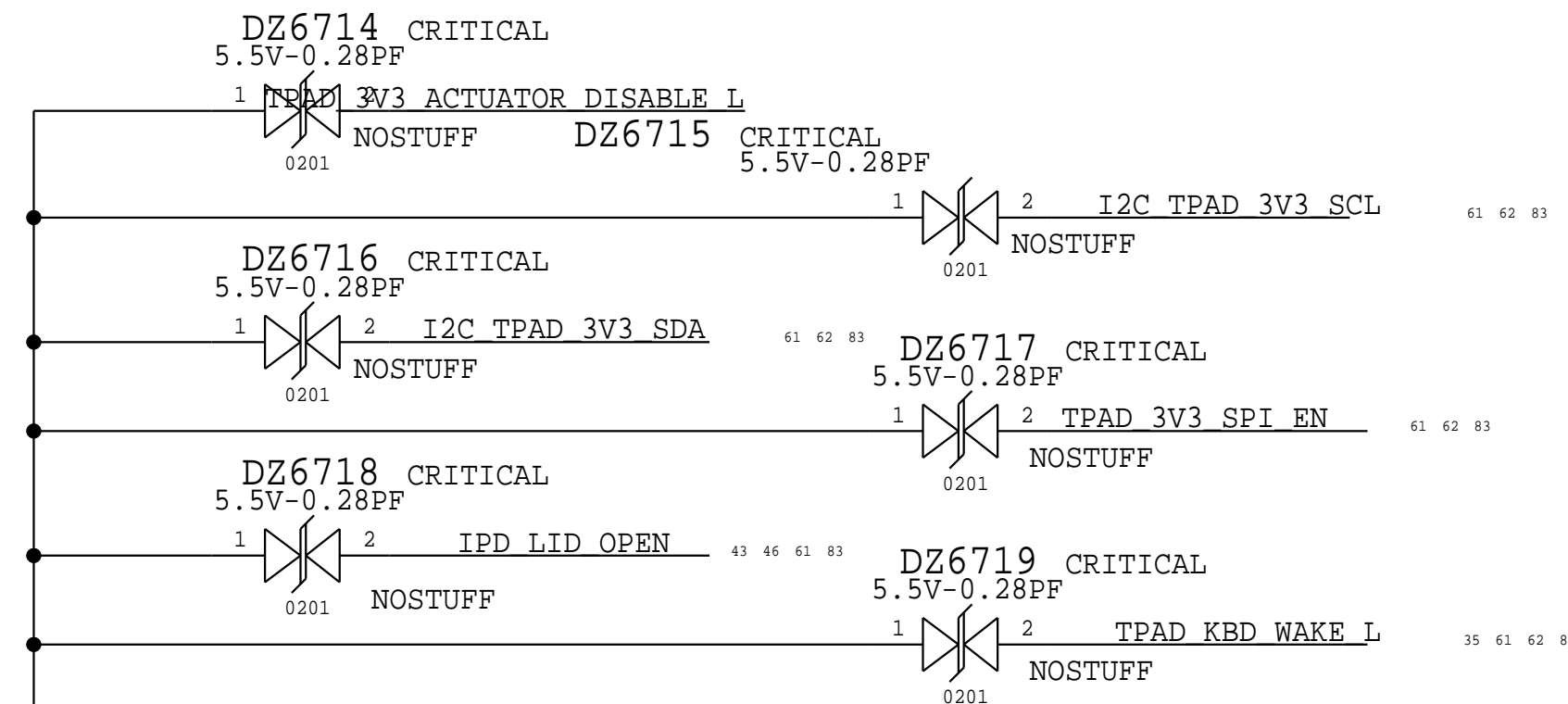
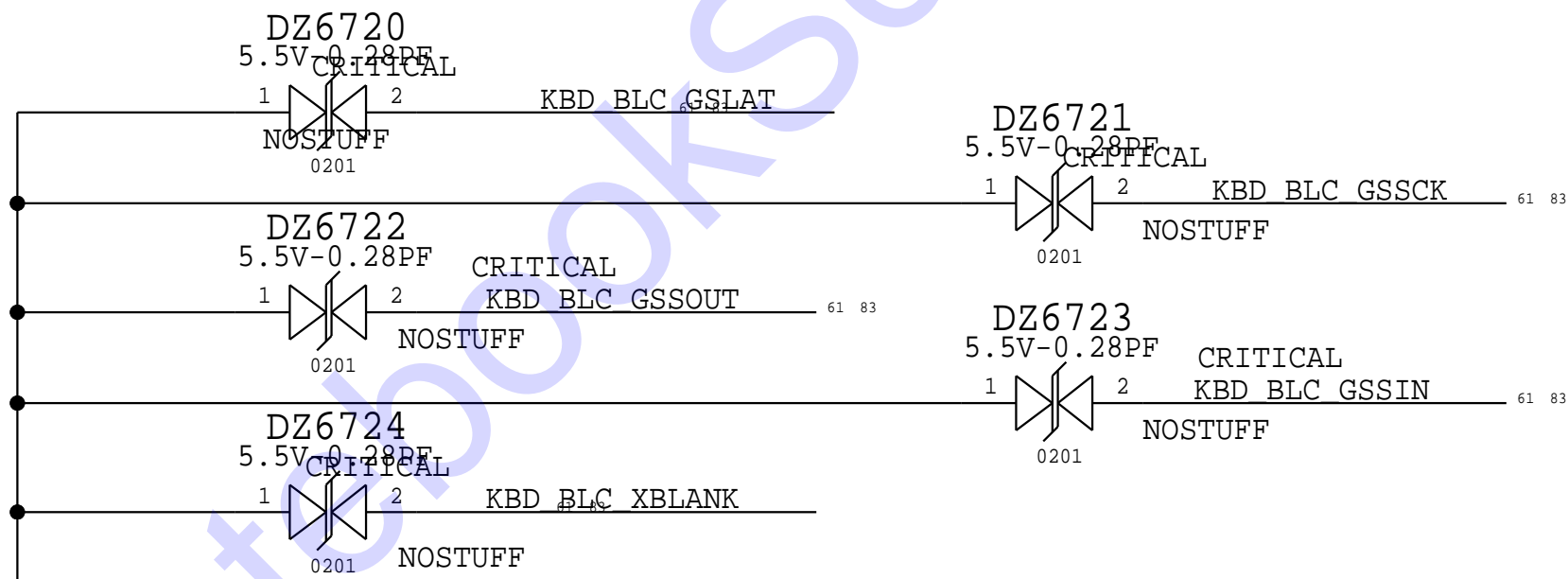
377S0184



TPAD CONNECTOR



516S00187, MATE WITH 516S00188



PAGE TITLE		
KEYBOARD & TRACKPAD 1		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	67 OF 500
	SHEET	61 OF 98

BOM_COST_GROUP=KEYBOARD

Trackpad Level Shifting

D

D

C

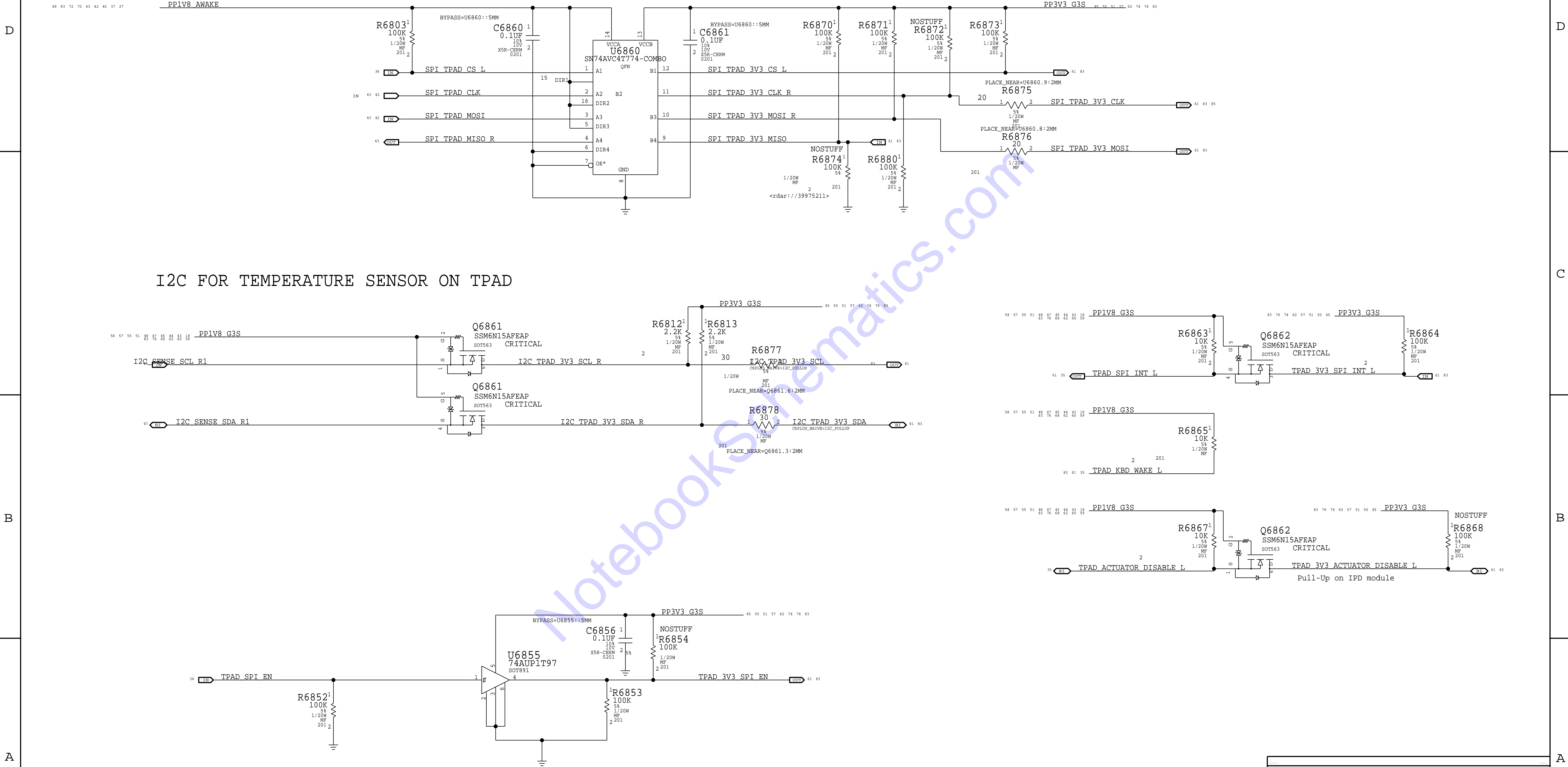
C


B

B

A

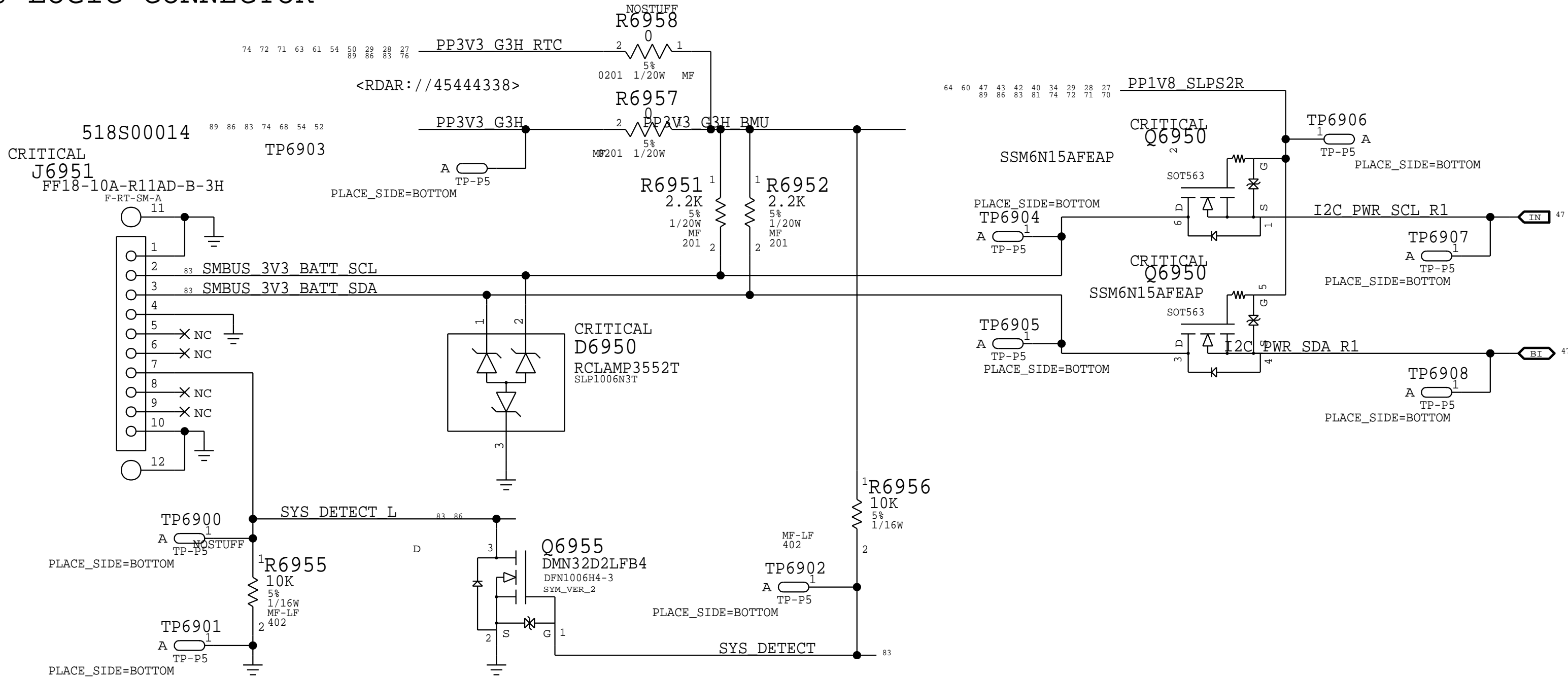
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PAGE TITLE		
KEYBOARD & TRACKPAD 2		
 Apple Inc.	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	68 OF 500
	SHEET	62 OF 98

BOM_COST_GROUP=TRACKPAD

BMU LOGIC CONNECTOR

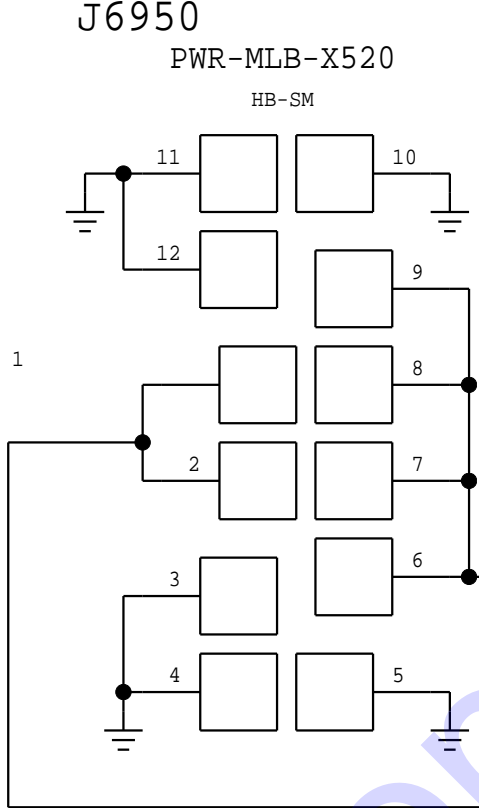


BATTERY (BMU) FLEX SOLDER PADS

BMU POWER FLEX IS SOLDERED TO MLB.

998-03828

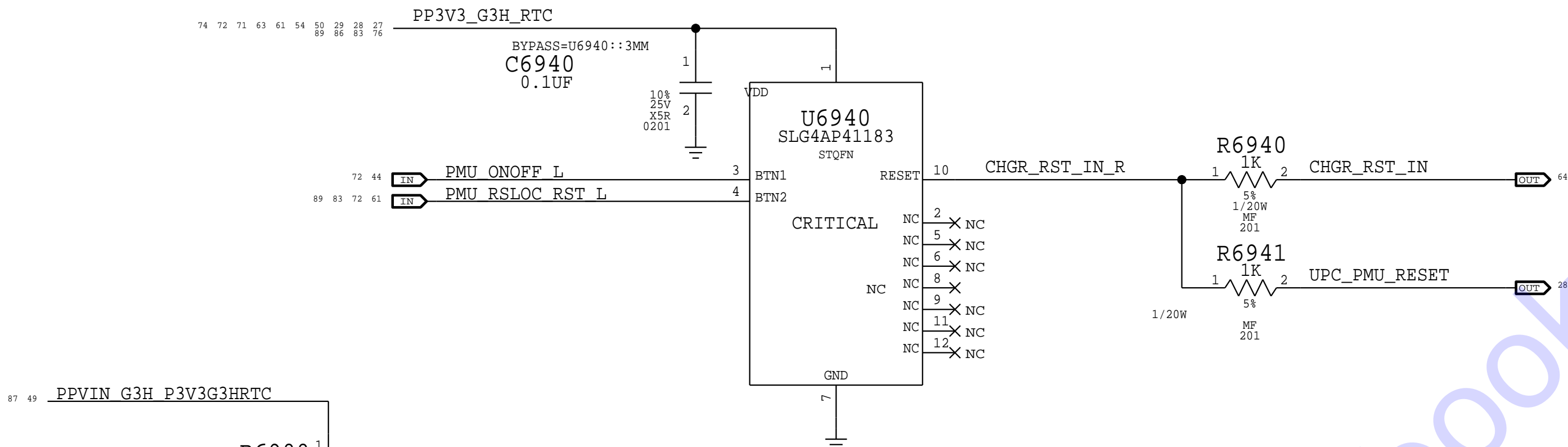
J6950



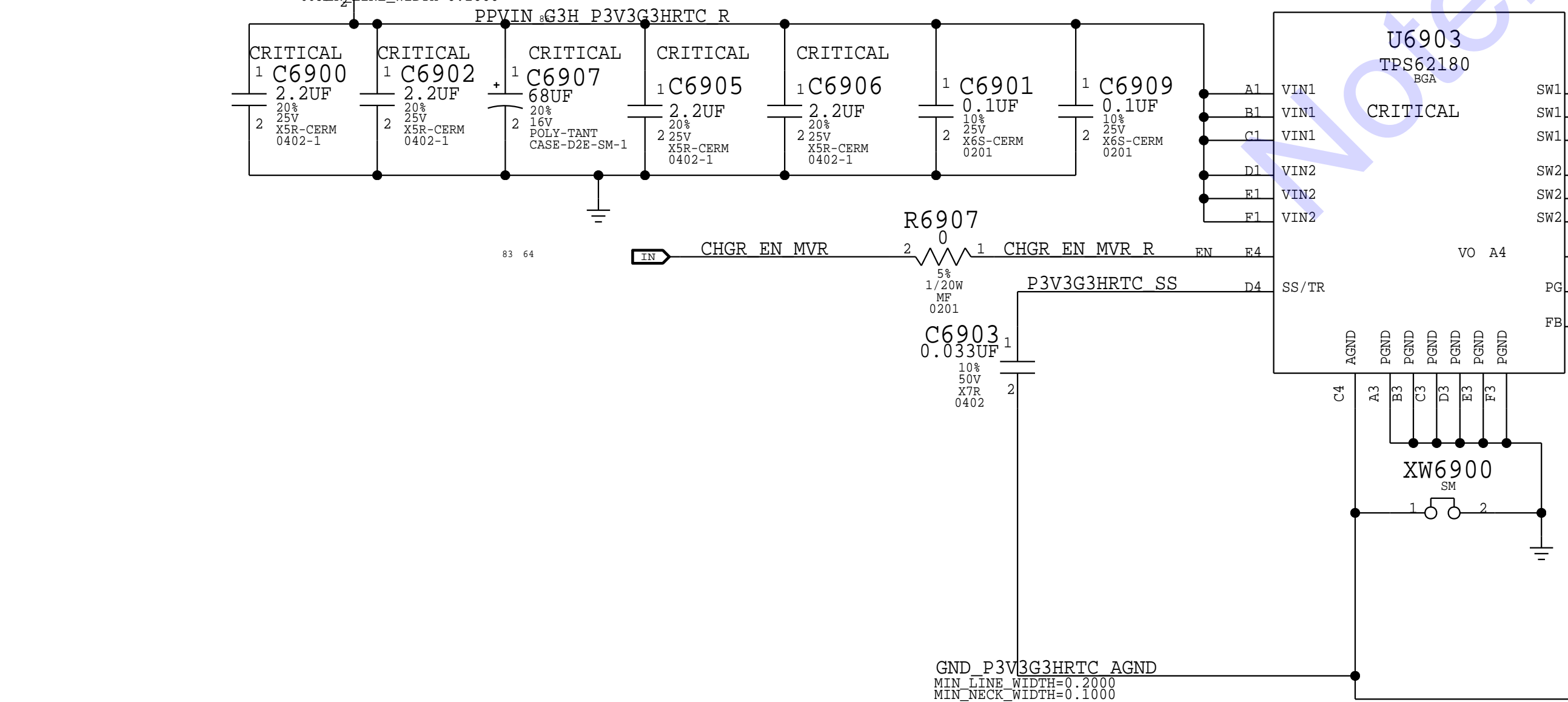
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	

SMC Reset Circuit

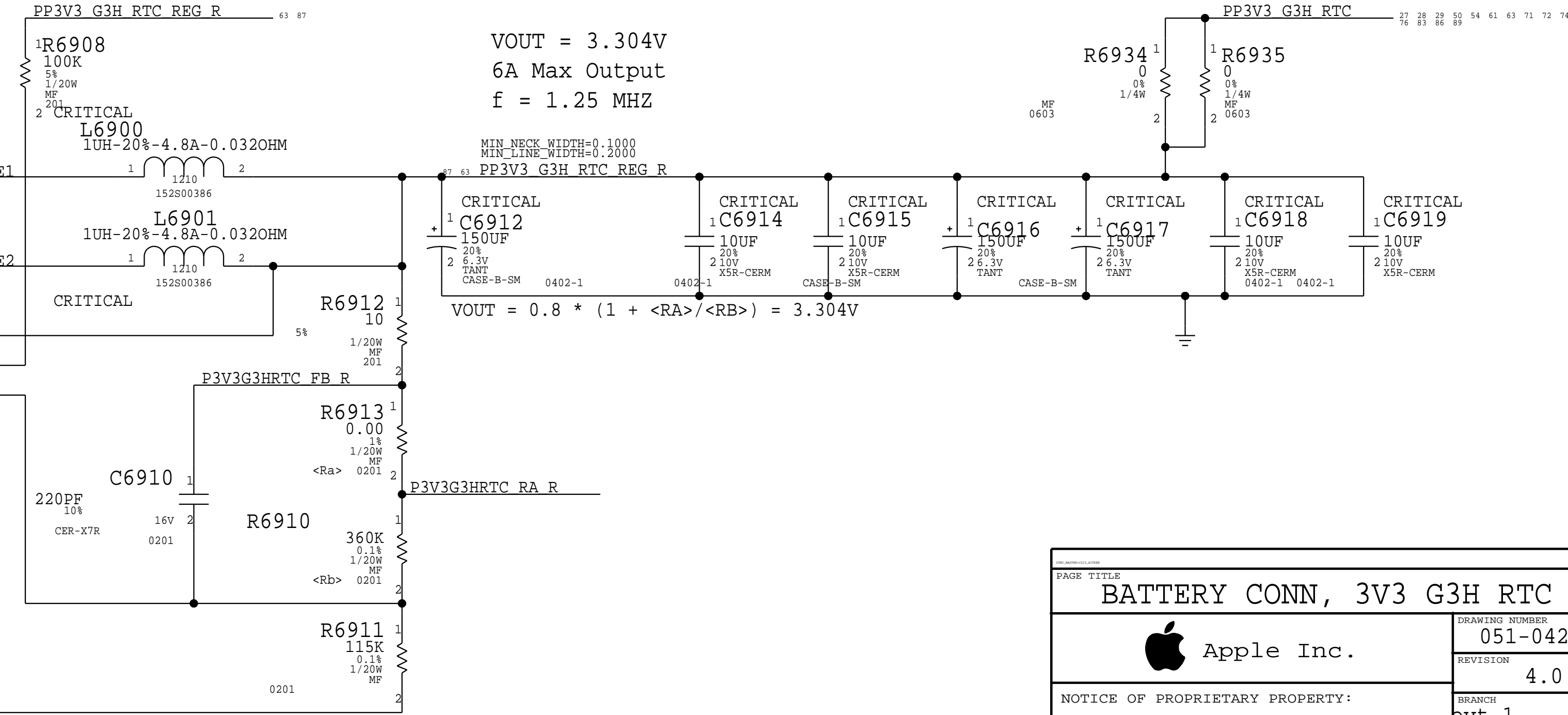
Right Shift & Left Option Control followed by ON OFF button press.



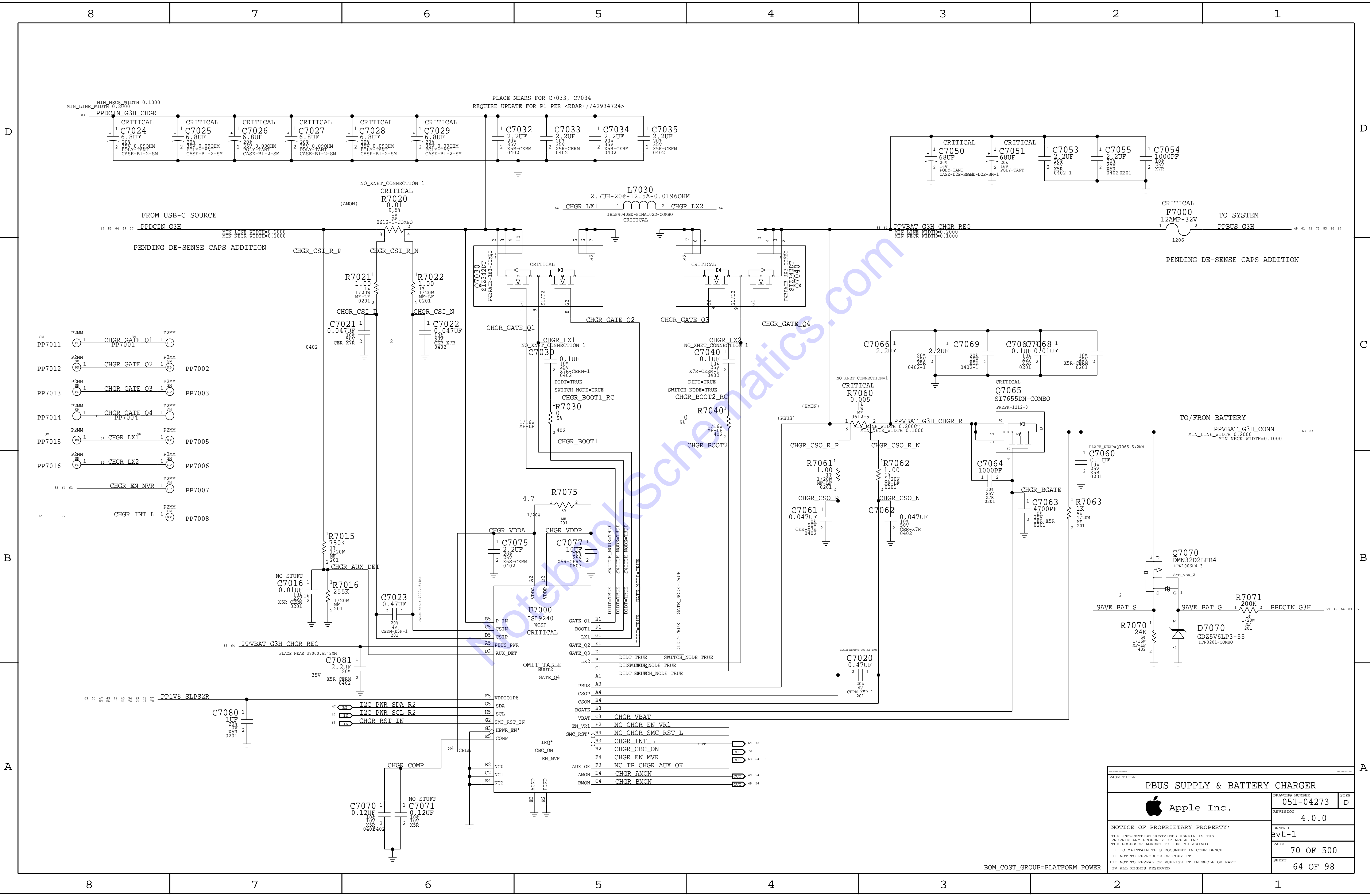
3.3V G3H RTC VR




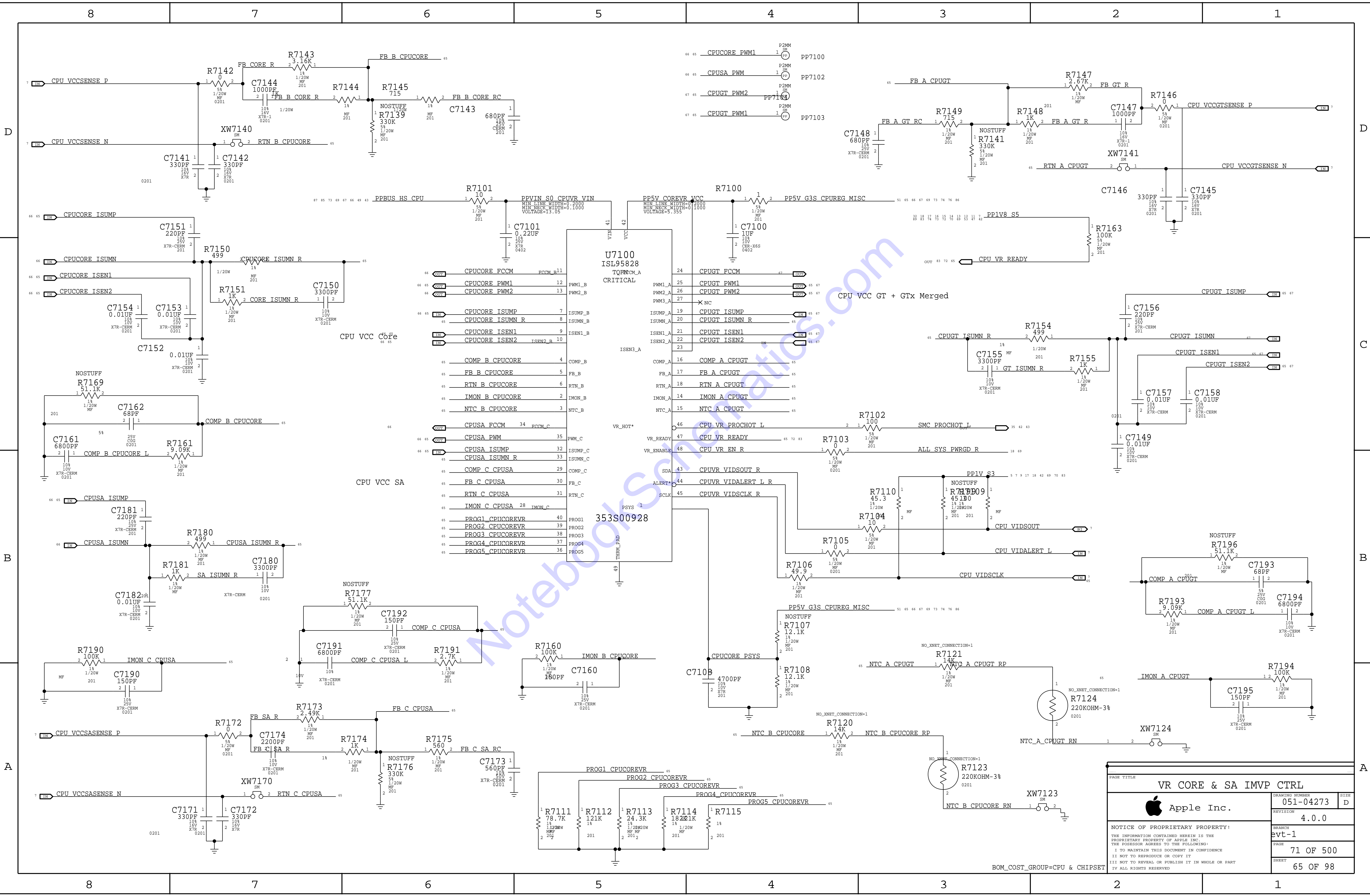
VOUT = 3.304V
6A Max Output
f = 1.25 MHZ




PAGE TITLE		
BATTERY CONN, 3V3 G3H RTC VR		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	69 OF 500
SHEET		63 OF 98

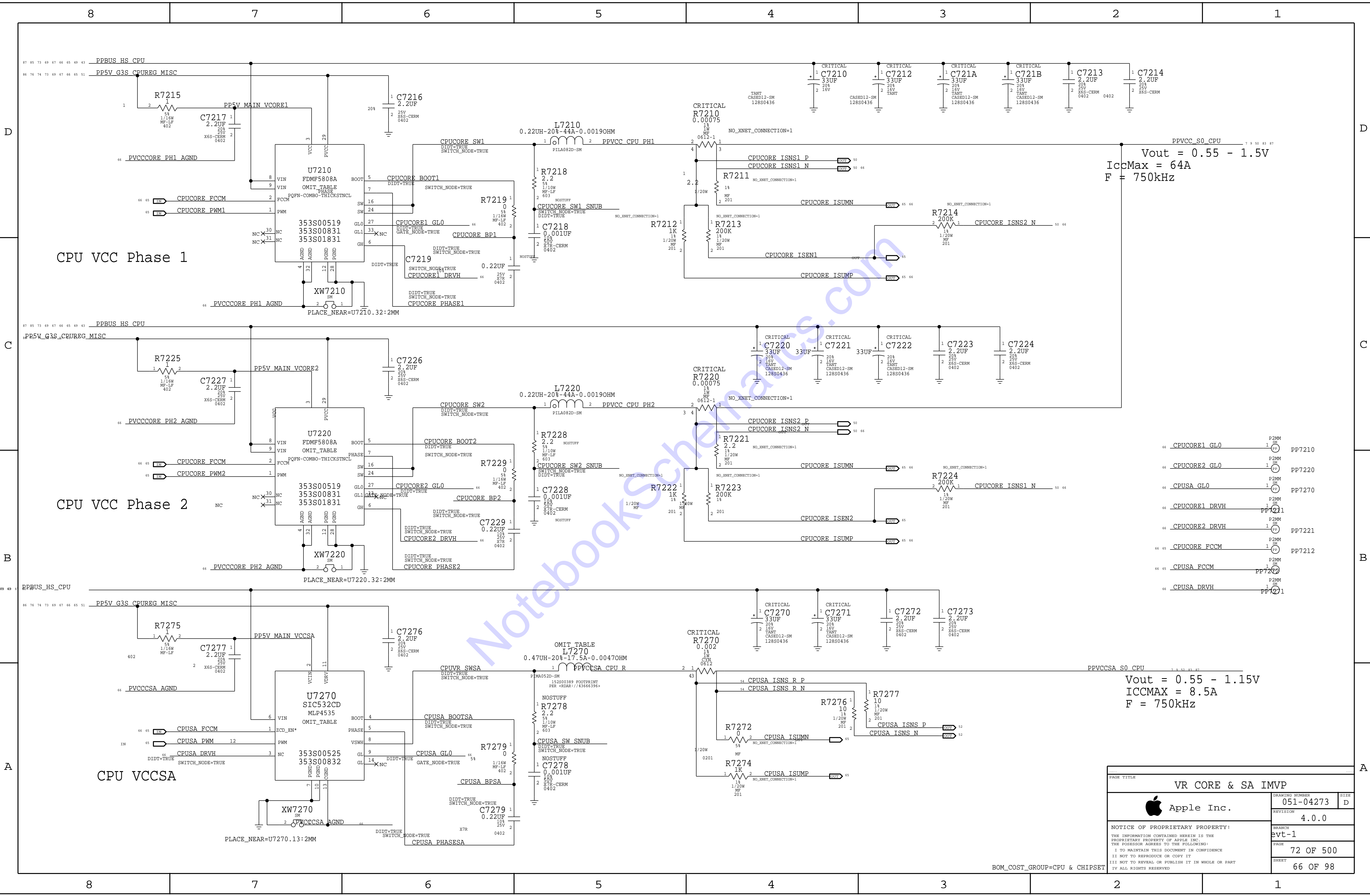


PAGE TITLE		
PBUS SUPPLY & BATTERY CHARGER		
 Apple Inc.	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	70 OF 500
	SHEET	64 OF 98



PAGE TITLE		
VR CORE & SA IMVP CTRL		
 Apple Inc.	DRAWING NUMBER	051-04273
	REVISION	4.0.0
	BRANCH	evt-1
	PAGE	71 OF 500
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		SHEET 65 OF 98

BOM_COST_GROUP=CPU & CHIPSET



Vout = 0.55 - 1.5V
IccMax = 64A
F = 750kHz

Vout = 0.55 - 1.15V
ICCMAX = 8.5A
F = 750kHz

PAGE TITLE		
VR CORE & SA IMVP		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	72 OF 500
	SHEET	66 OF 98

BOM_COST_GROUP=CPU & CHIPSET

D

B

A

D

C

B

A

8

7

6

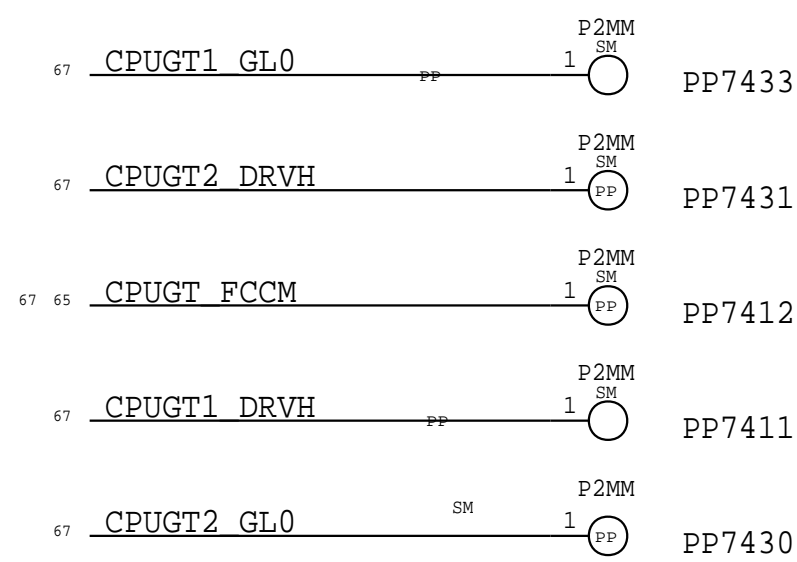
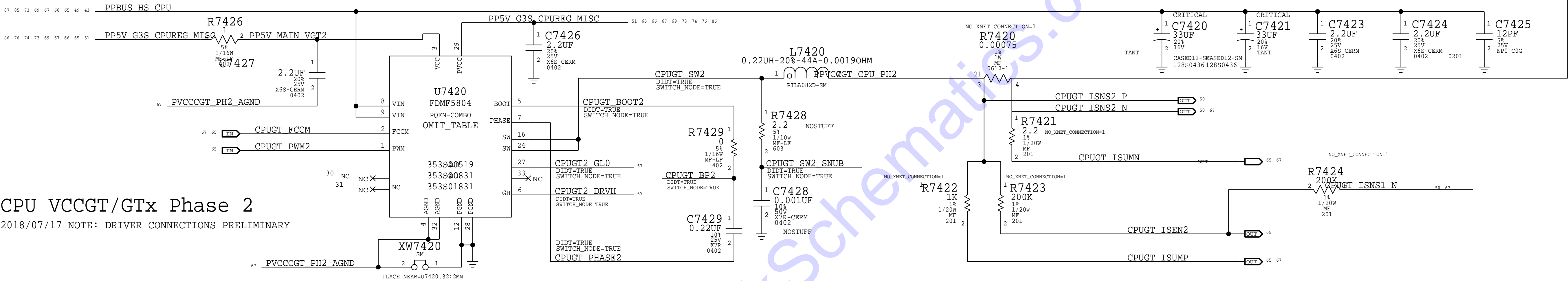
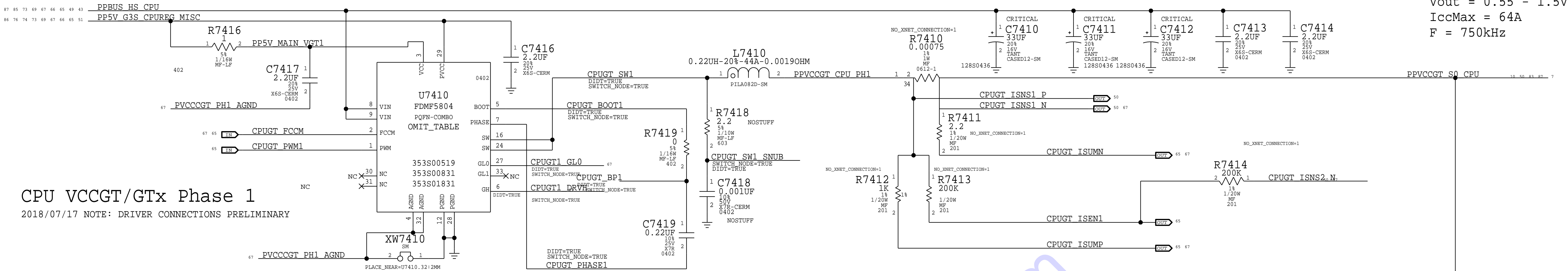
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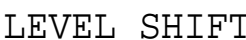
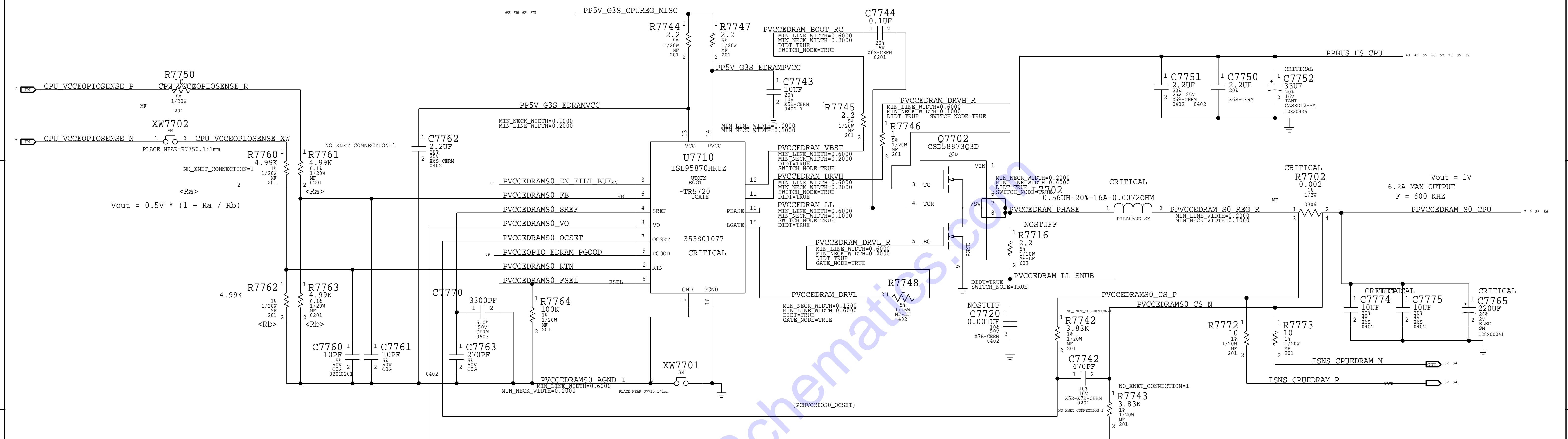
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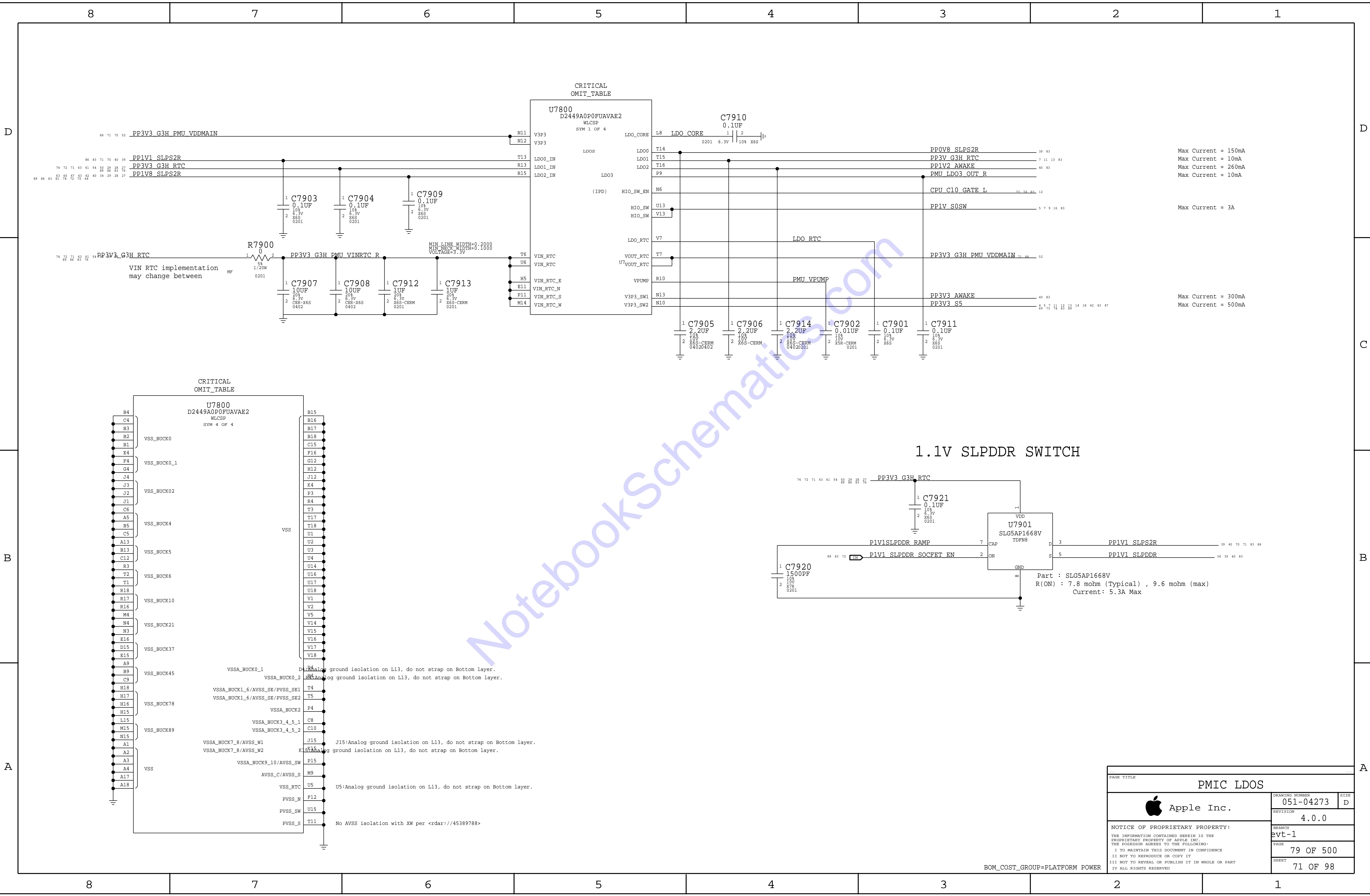
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE		
VR GT & GTX IMVP		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED	BRANCH	evt-1
	PAGE	74 OF 500
	SHEET	67 OF 98



BOM_COST_GROUP=CPU & CHIPSET


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VR EOPIO EDRAM			
 Apple Inc.	DRAWING NUMBER 051-04273		SIZE D
	REVISION 4.0.0		
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		SHEET 69 OF 98	



PAGE TITLE		
PMIC LDOS		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	79 OF 500
	SHEET	71 OF 98

BOM_COST_GROUP=PLATFORM POWER



PAGE TITLE			
PMIC GPIOs & CONTROL			
 Apple Inc.	DRAWING NUMBER	051-04273	SIZE D
	REVISION	4.0.0	
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		SHEET	72 OF 98

D

B

A

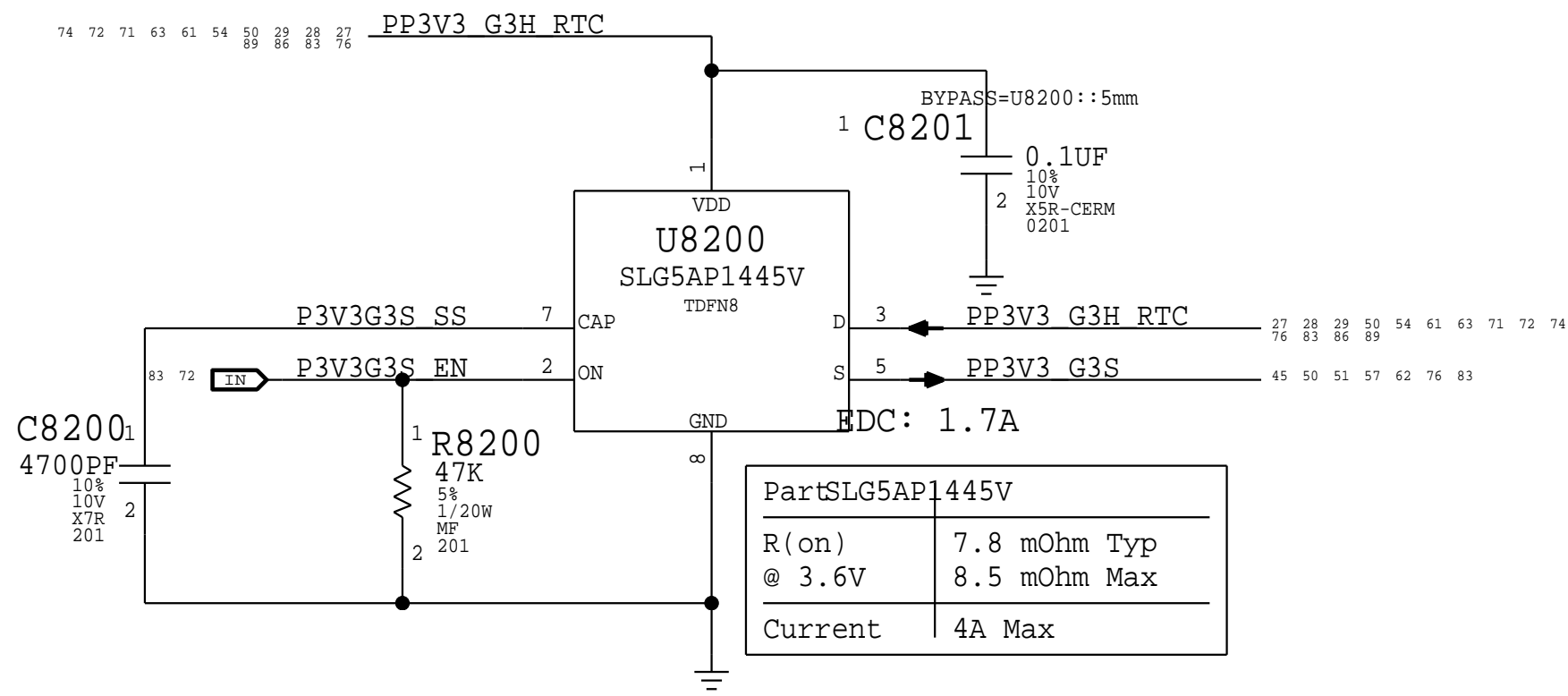
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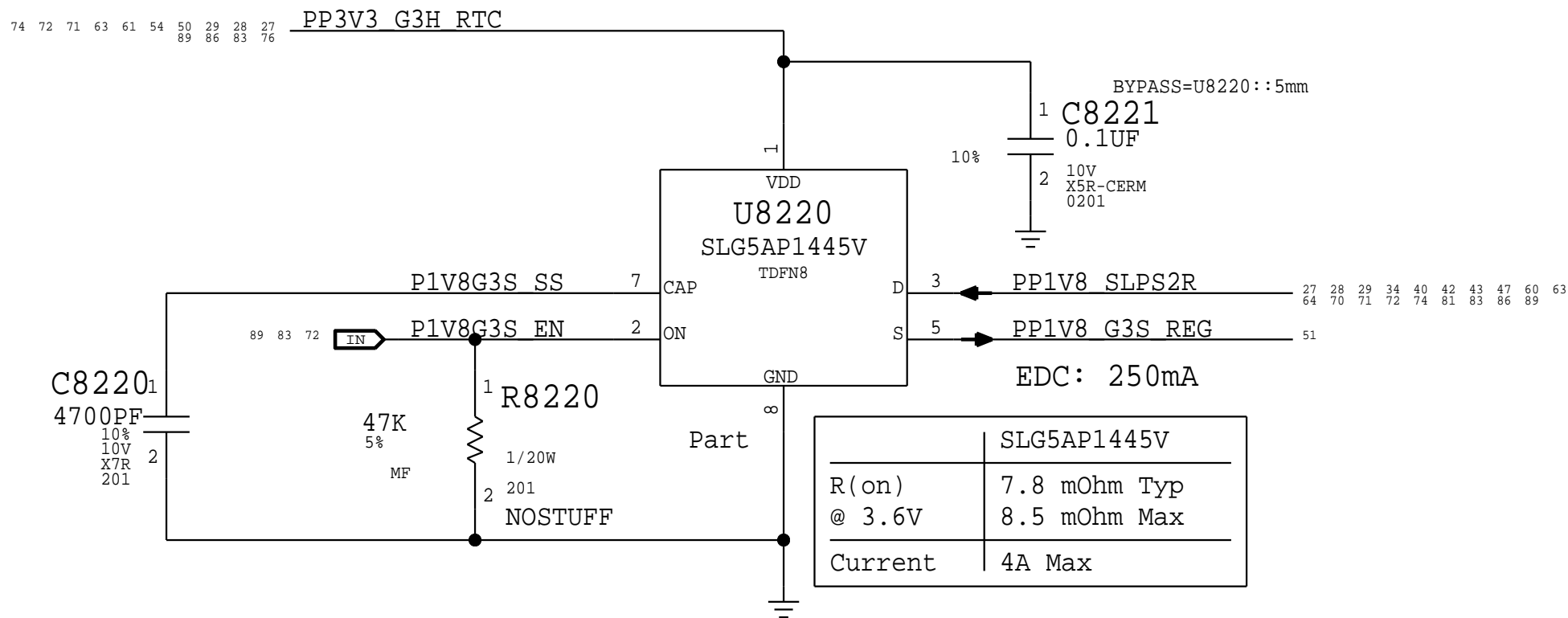
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A

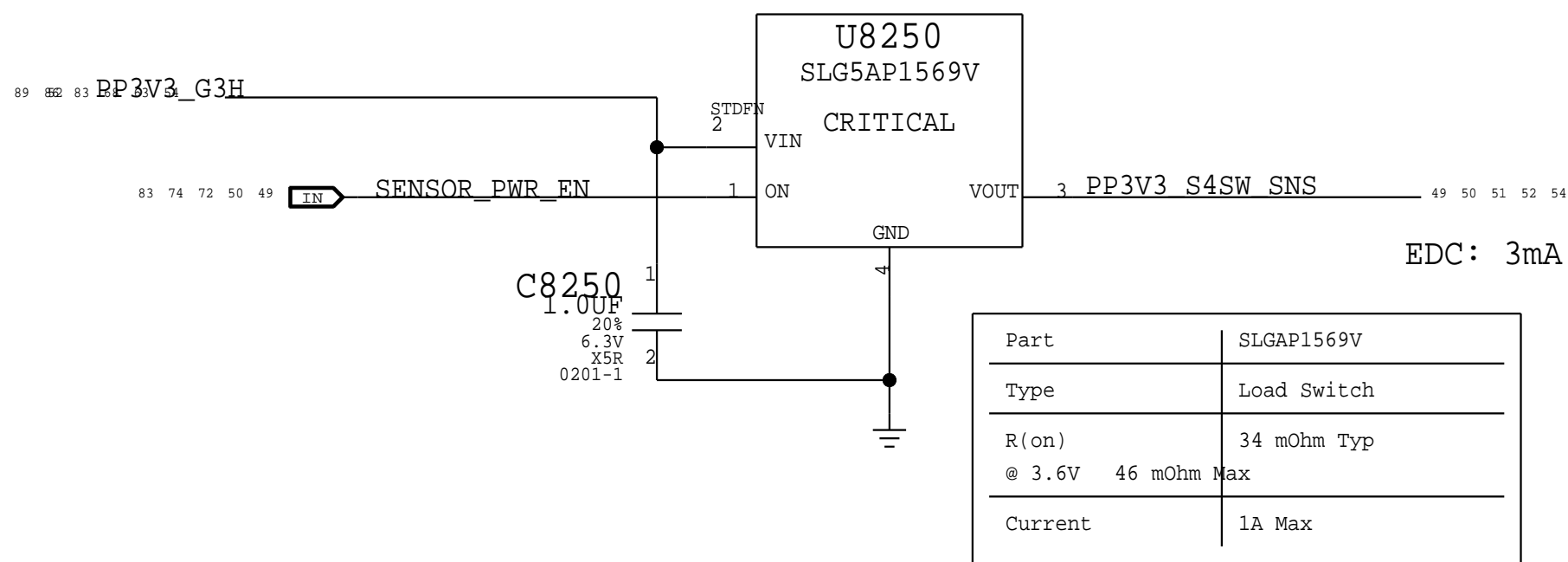
3.3V G3 Standby Switch



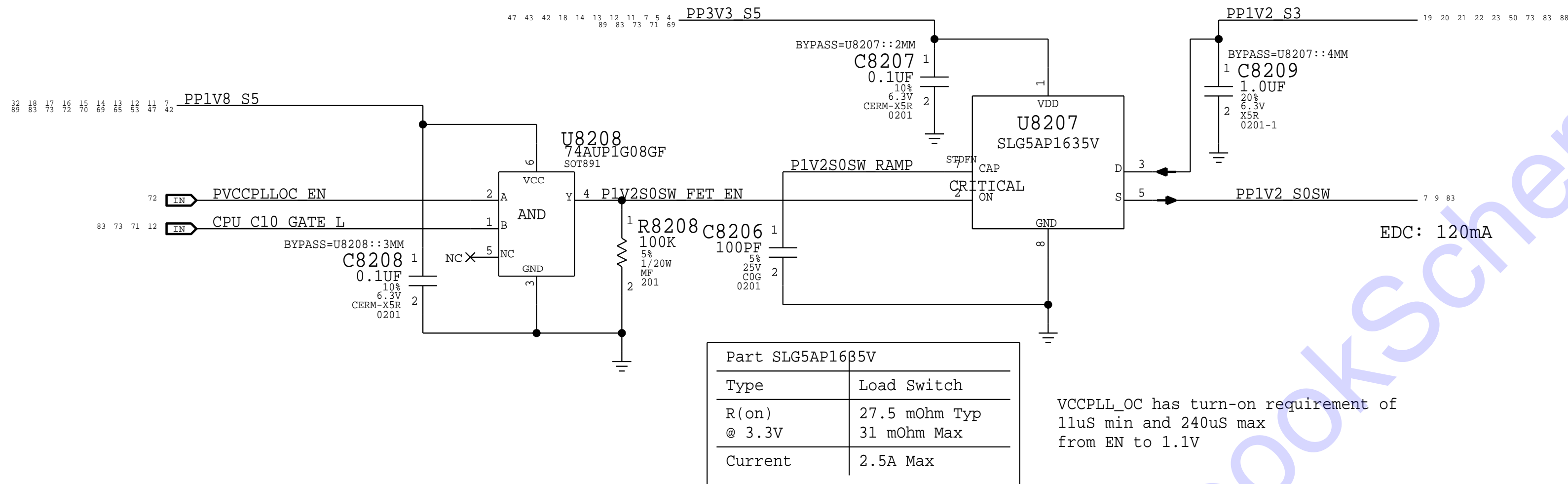
1.8V G3 Standby Switch



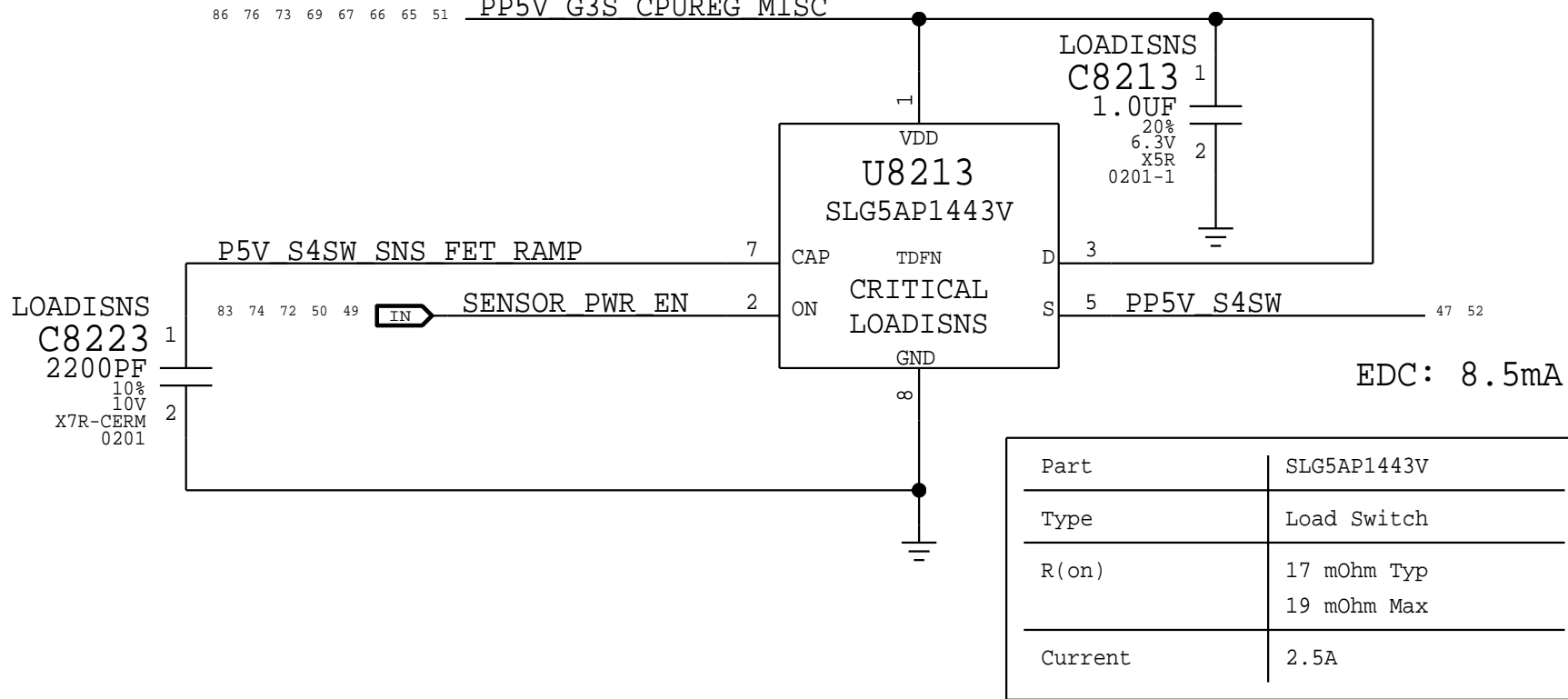
3.3V Sensor Switch



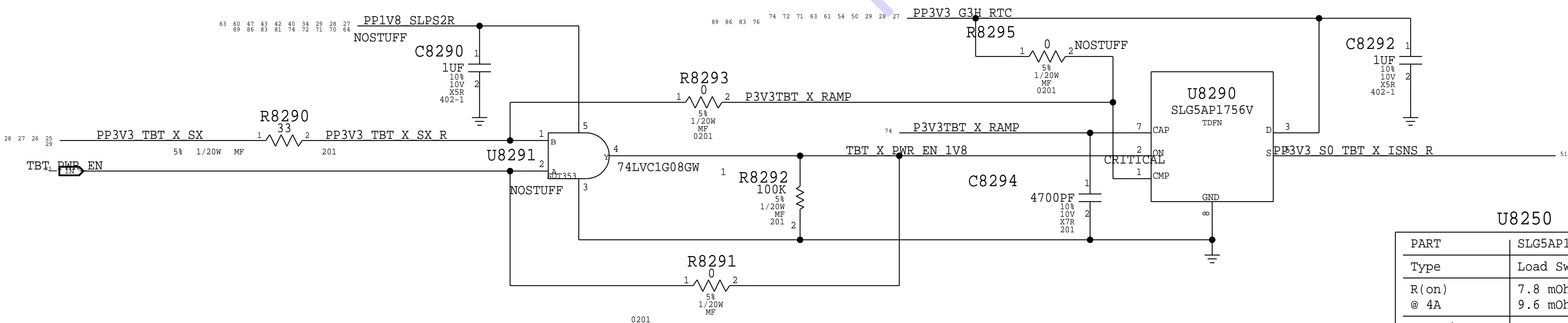
1.2V S0SW VCCPLL_OC Switch



5V Sensor Switch



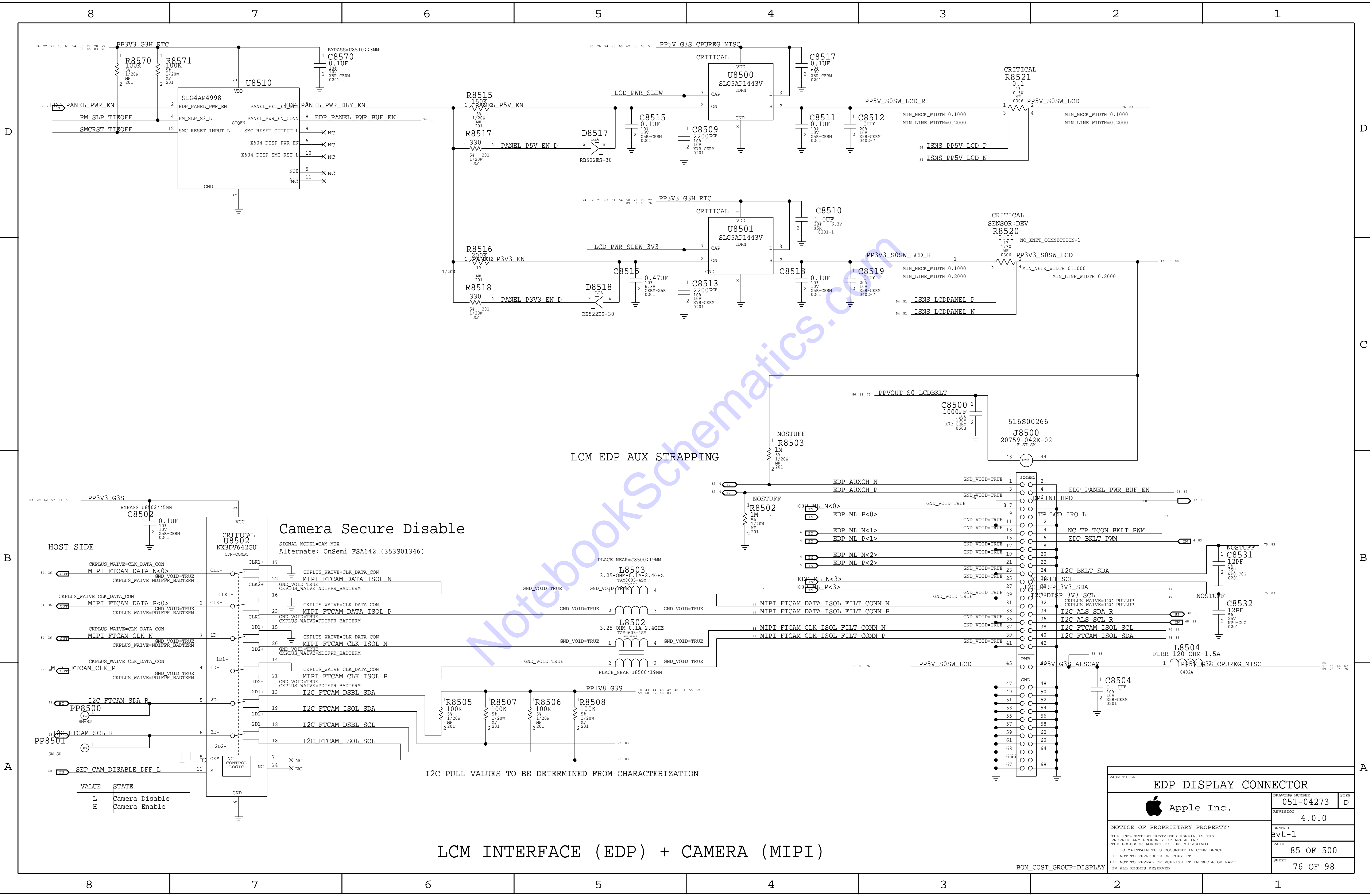
3.3V S0SW TBT X Switch



U8250	
Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ 9.6 mOhm Max
Current	4A Max

Power FETs		
	DRAWING NUMBER	051-04273
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	PAGE	82 OF 500
SHEET		74 OF 98

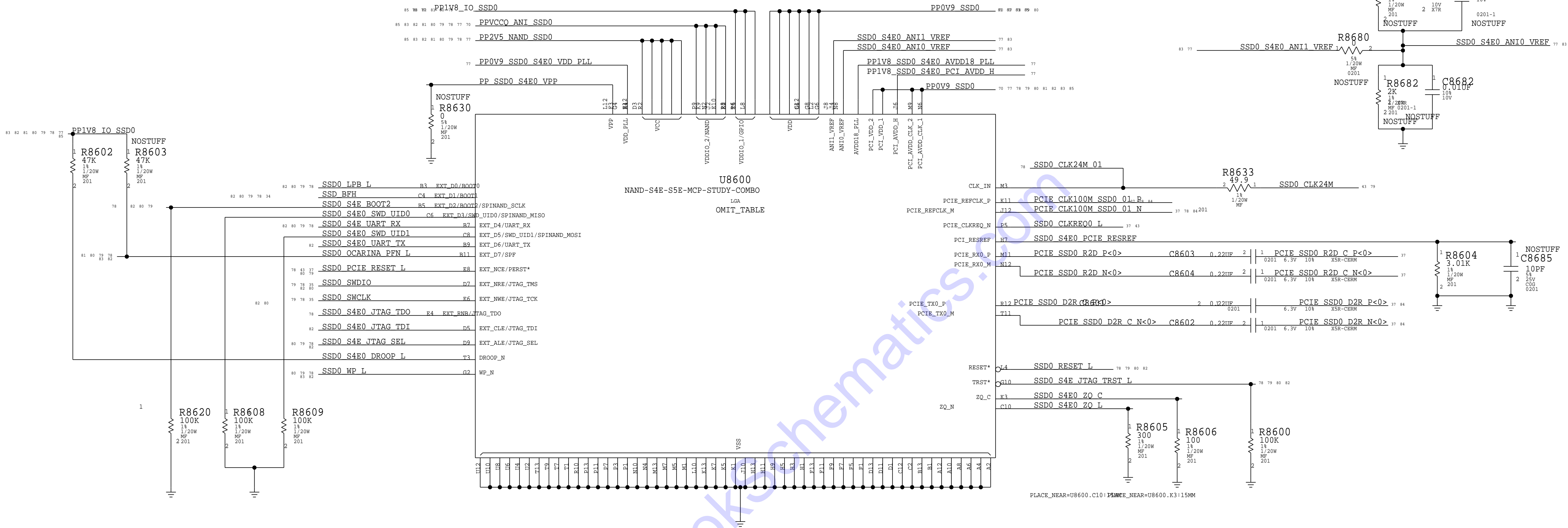
BOM_COST_GROUP=PLATFORM_POWER



I2C PULL VALUES TO BE DETERMINED FROM CHARACTERIZATION

BOM_COST_GROUP=DISPLAY

S4E0



S4E VDD

S4E VDDIO_2

S4E VDDIO_1

VCC CAP

EXTERNAL VREF

S4E<0>



Apple Inc.

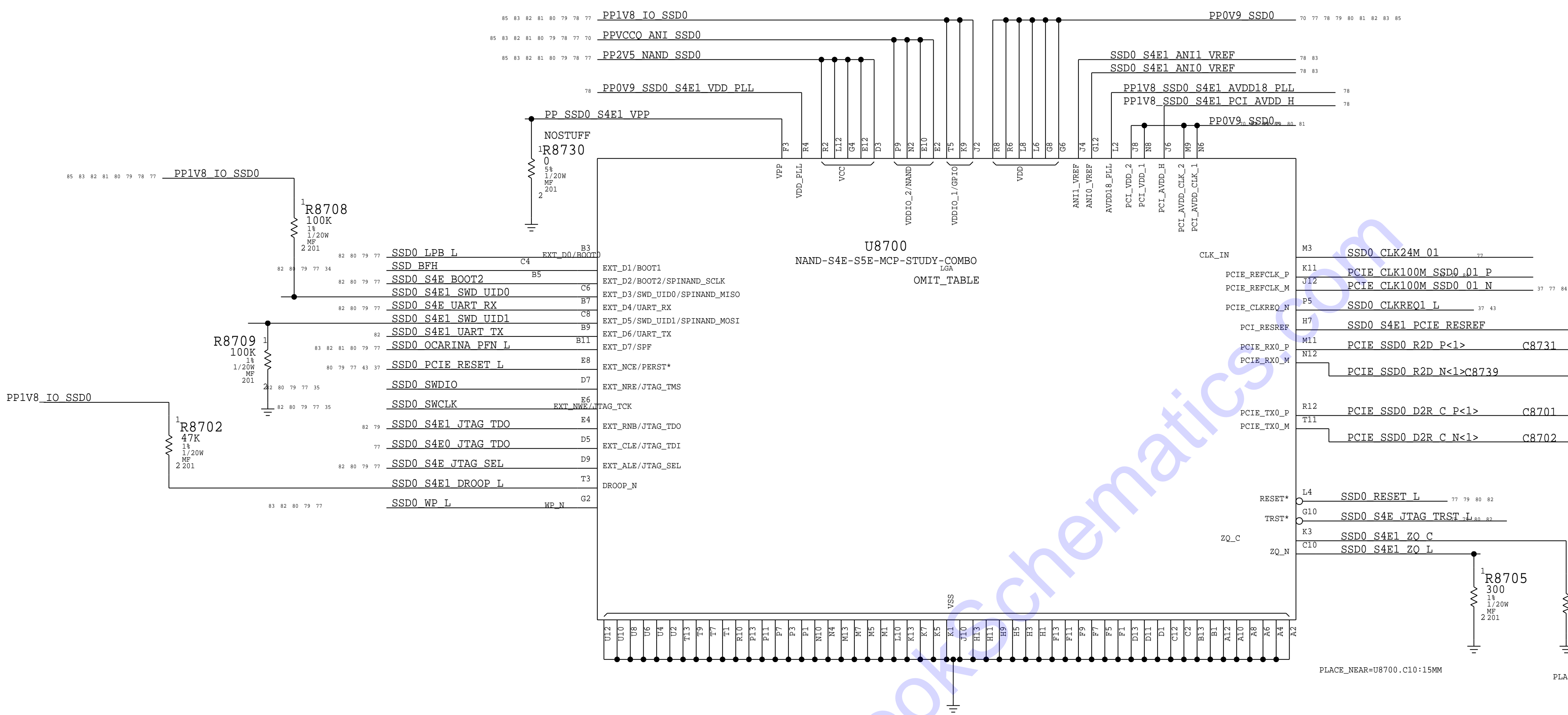
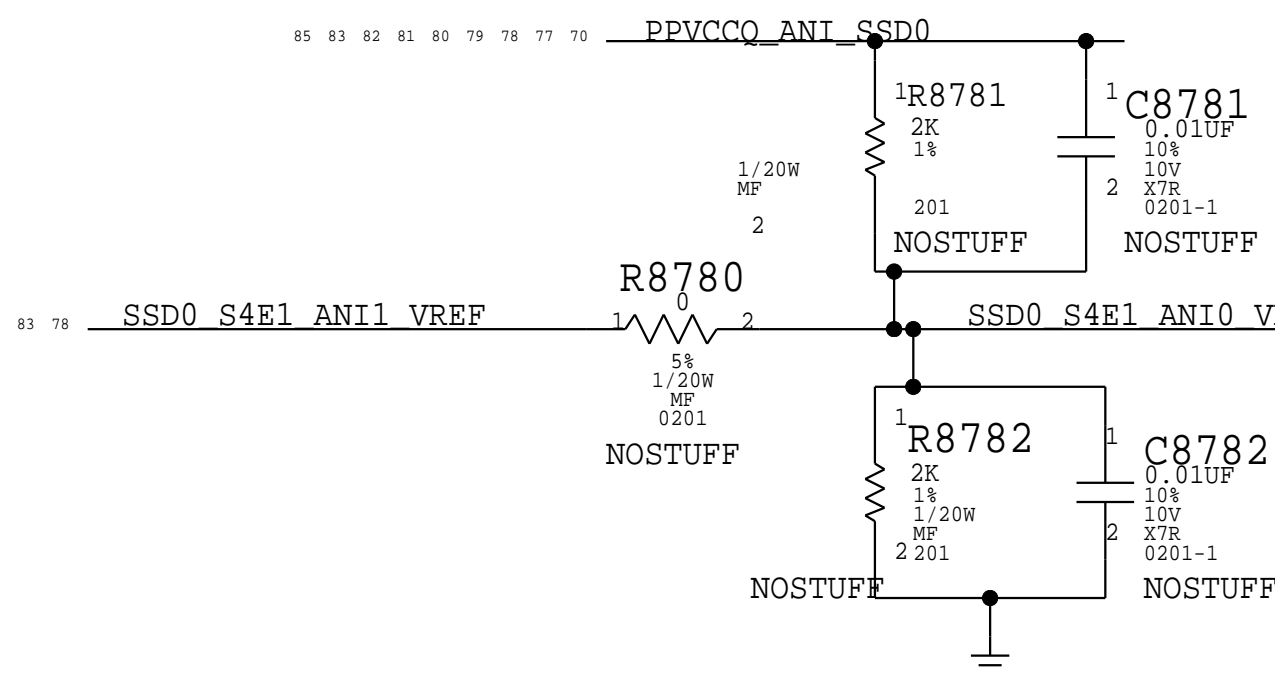
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DRAWING NUMBER	051-04273	SIZE	D
REVISION	4.0.0		
BRANCH	evt-1		
PAGE	86 OF 500		
SHEET	77 OF 98		

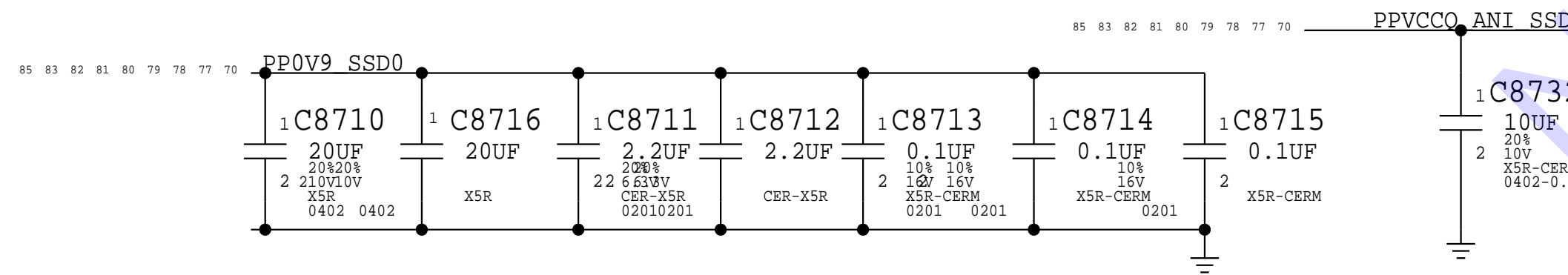
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S4E1

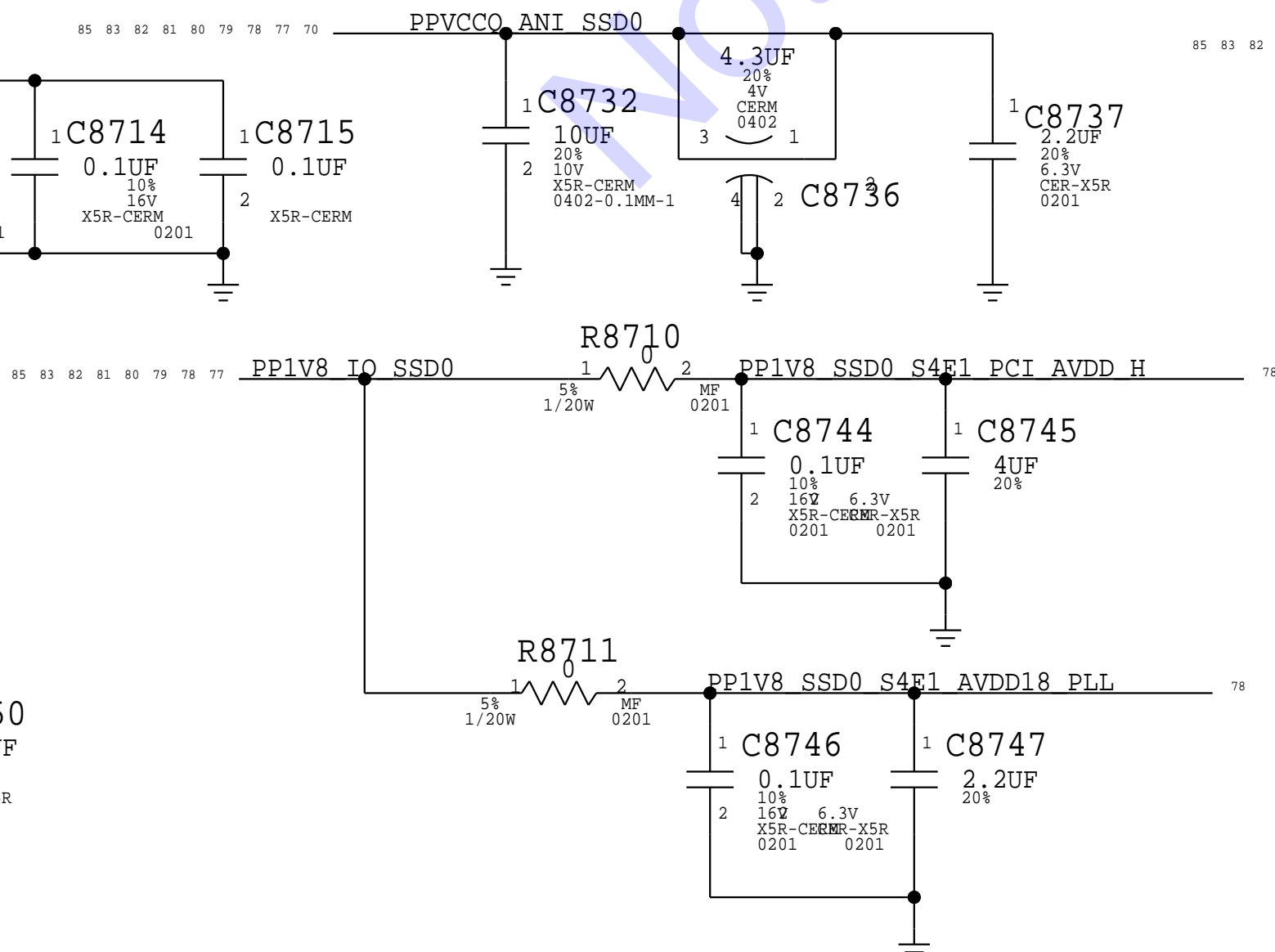
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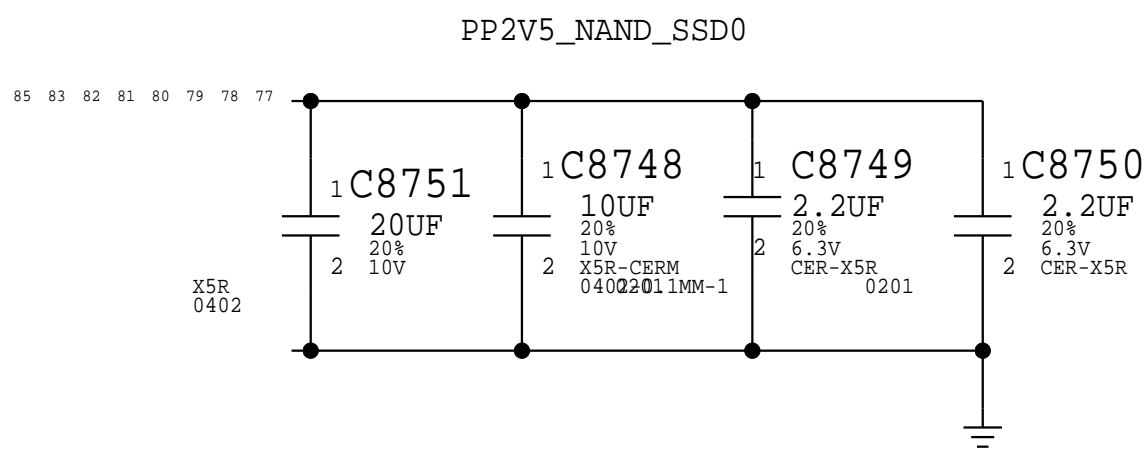
S4E VDD



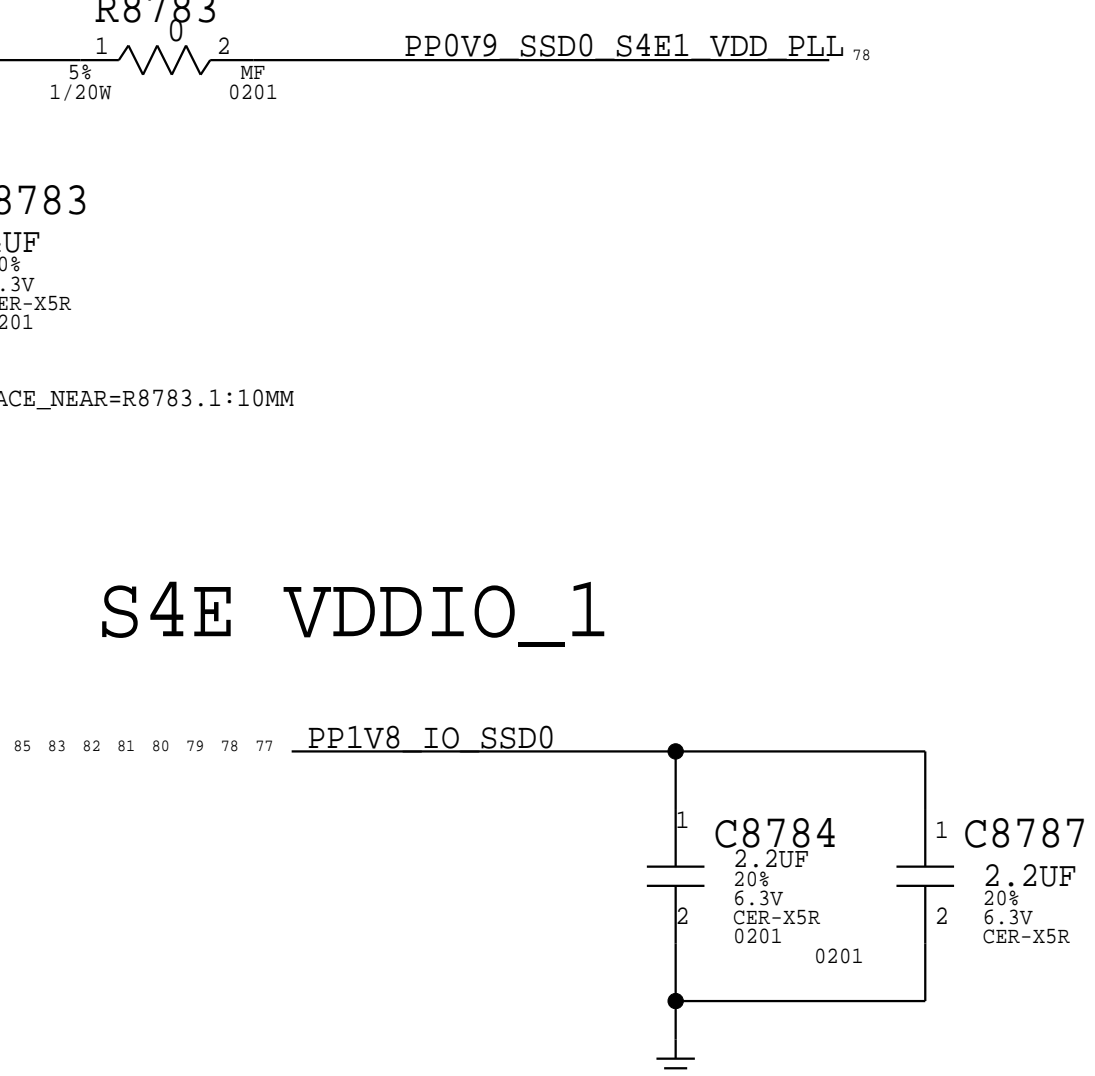
S4E VDDIO_2



VCC CAP

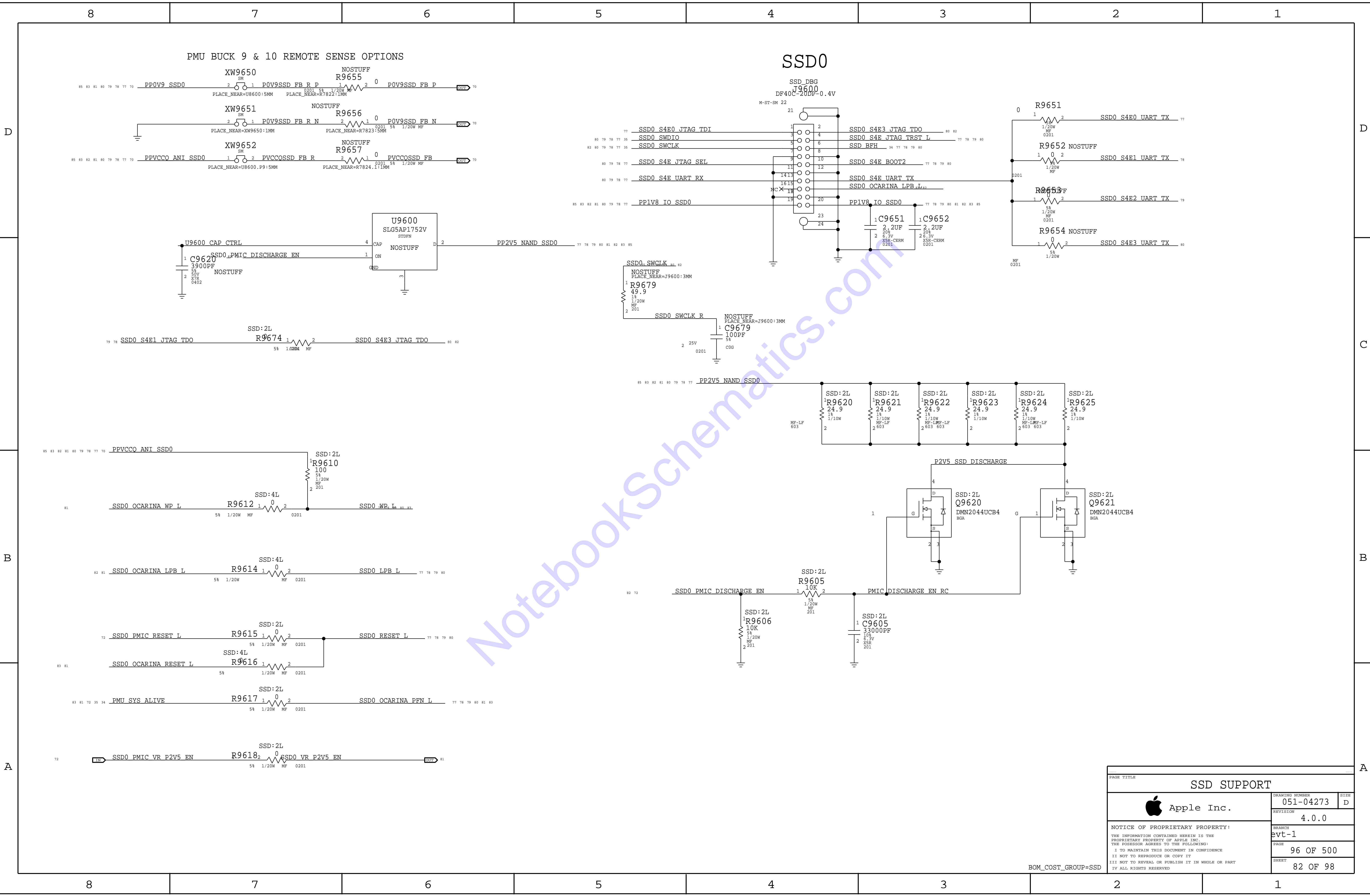


S4E VDDIO_1



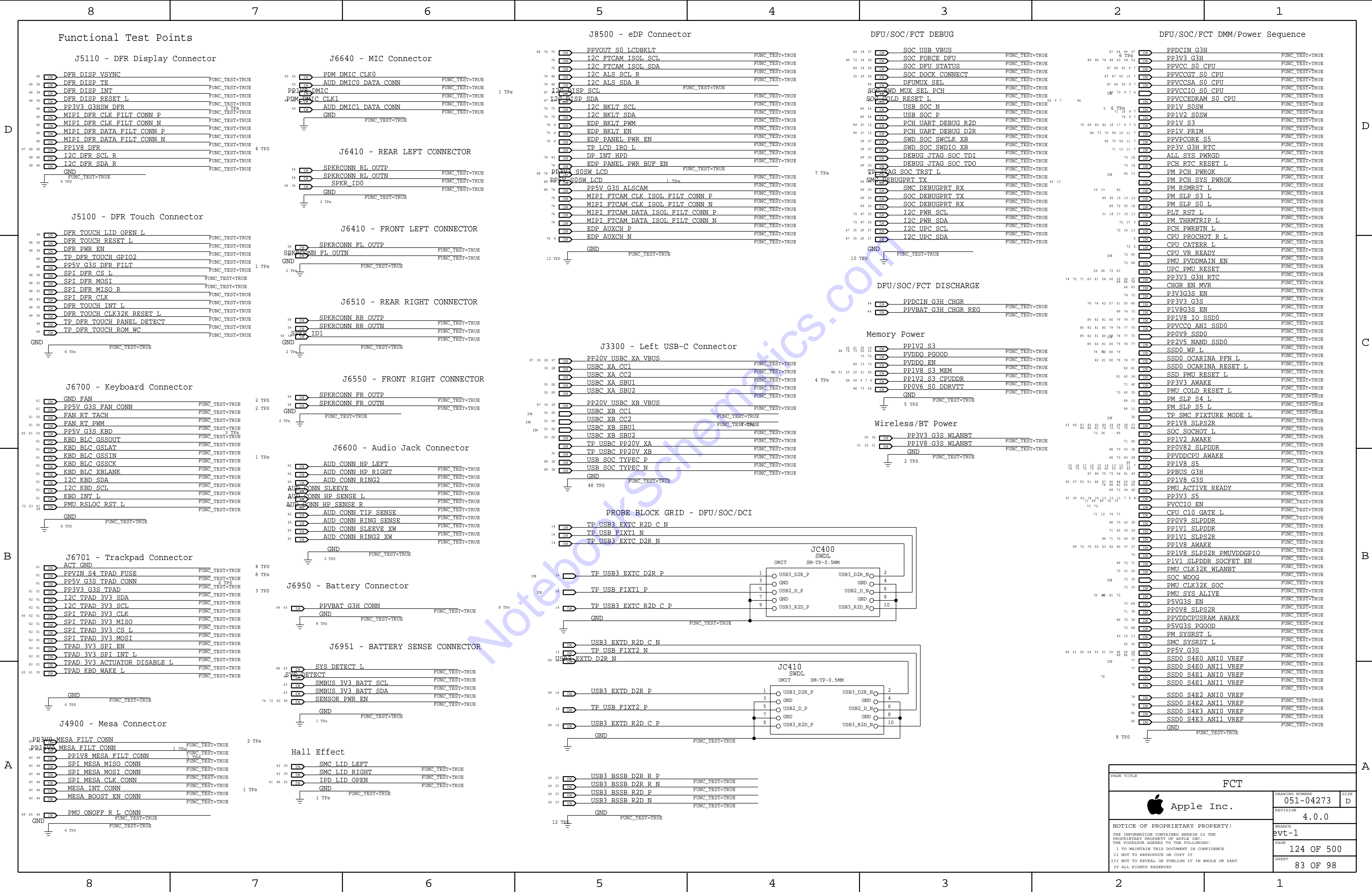
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	PAGE	87 OF 500
	SHEET	78 OF 98

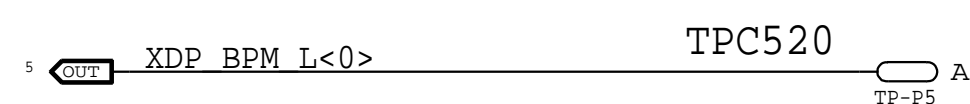
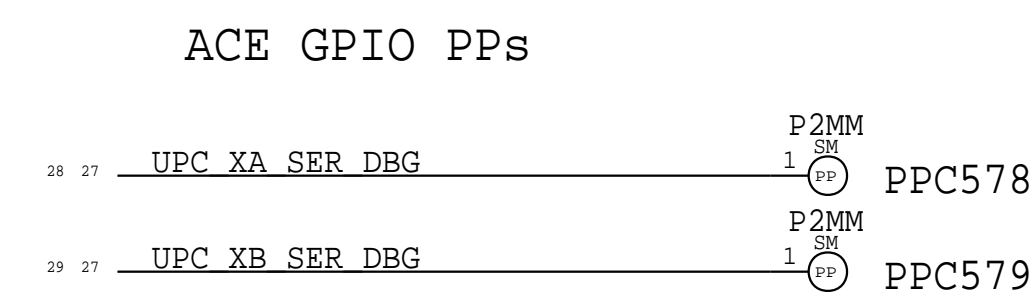
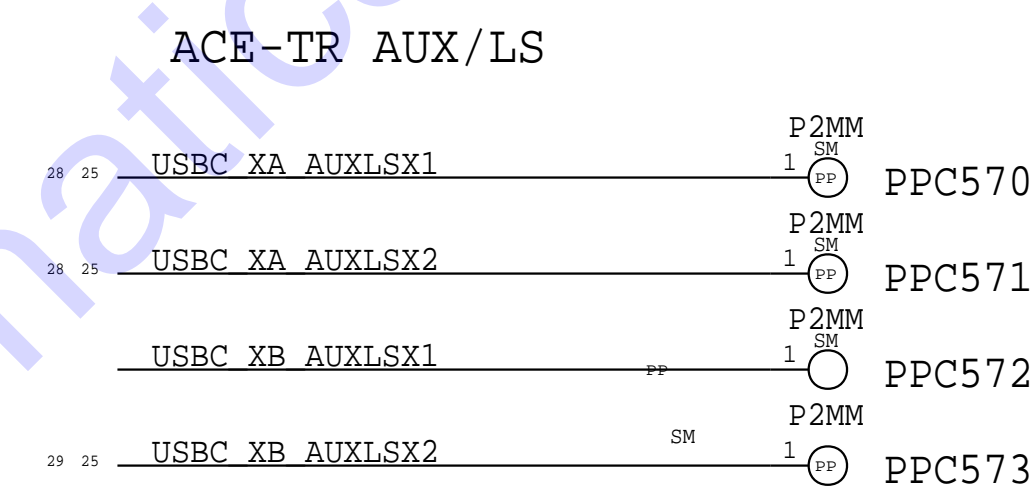
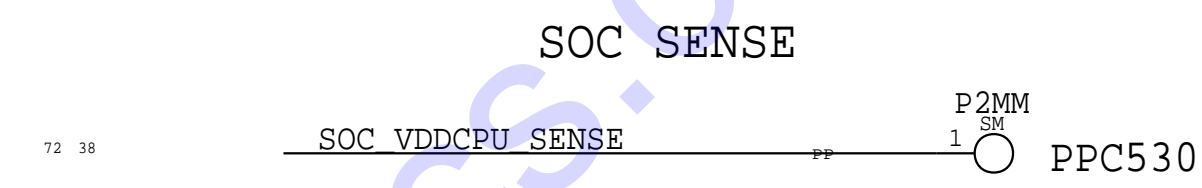
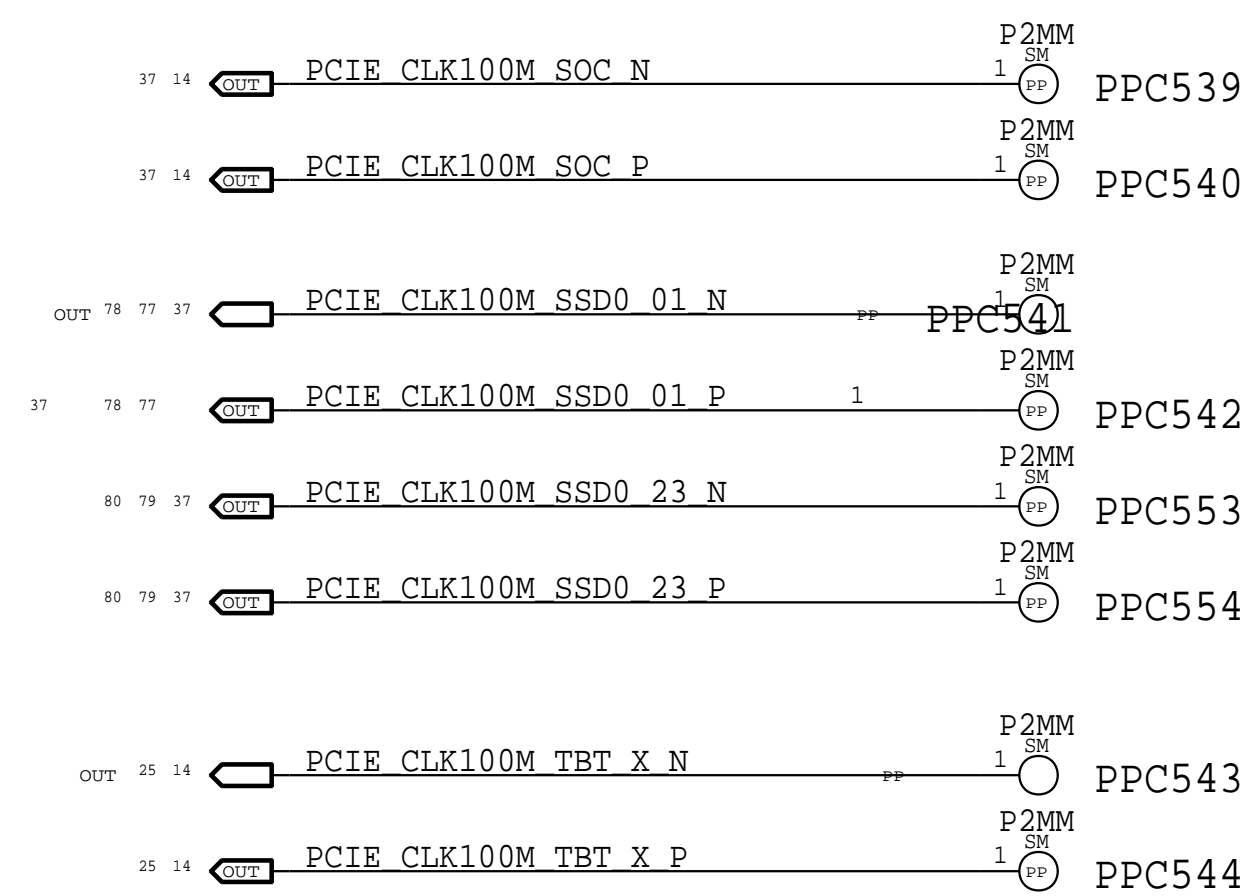
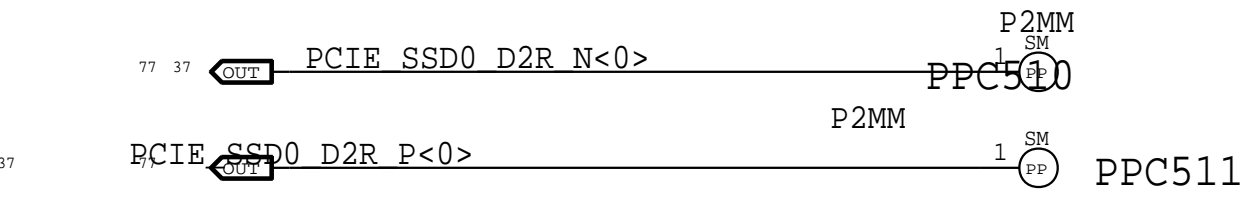
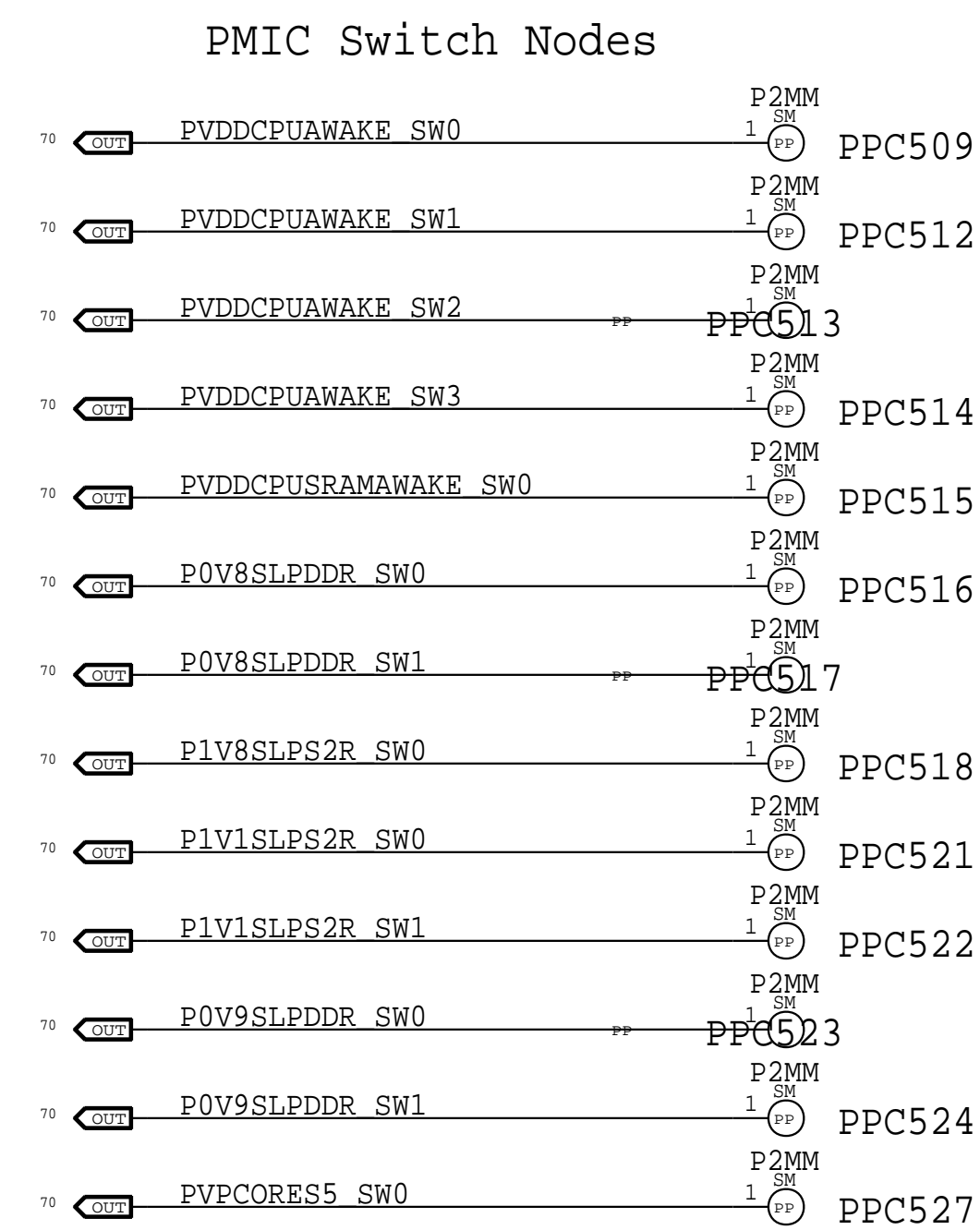
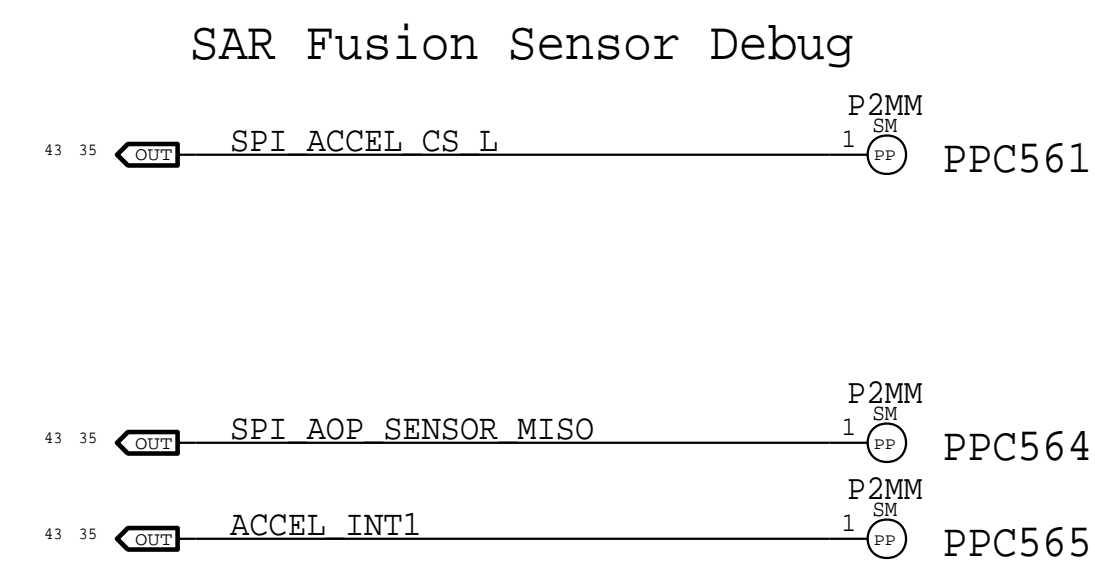
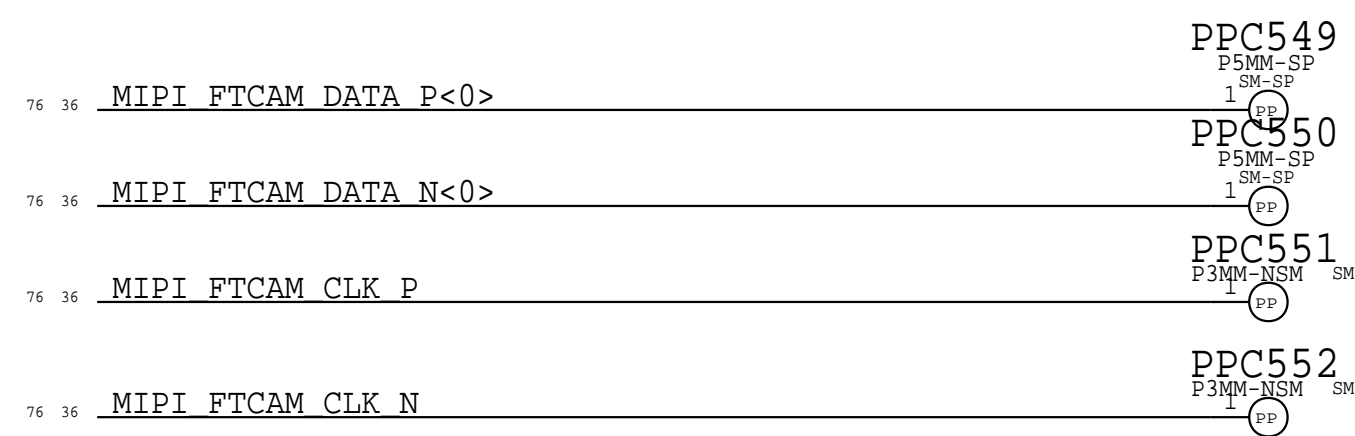
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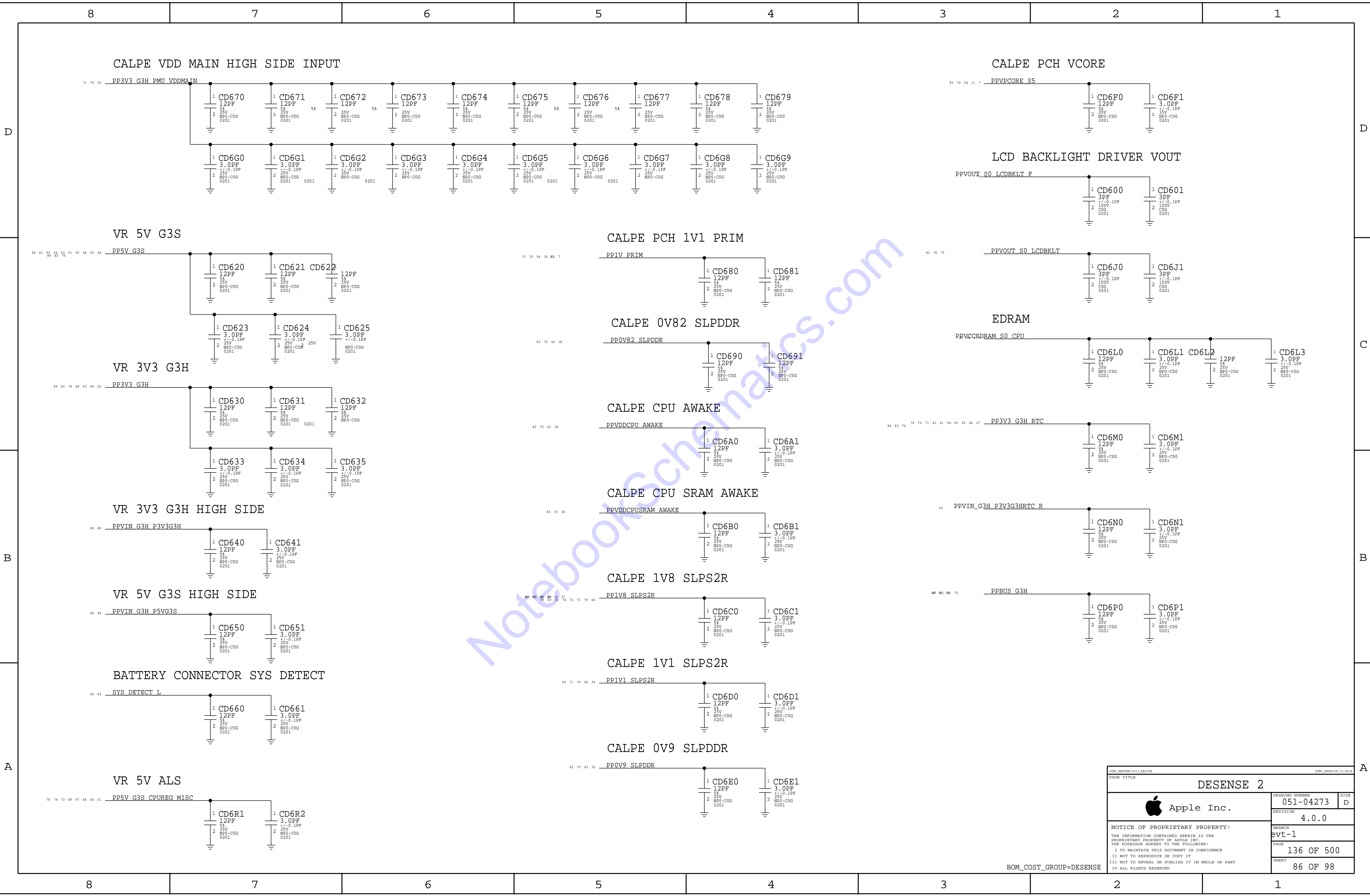
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SSD SUPPORT		
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	REVISION	4.0.0
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	PAGE	96 OF 500
	SHEET	82 OF 98

BOM_COST_GROUP=SSD






PAGE TITLE			
<div>PROBE POINTS</div>			
 <div>Apple Inc.</div>	<div>DRAWING NUMBER</div> <div>051-04273</div>		<div>SIZE</div> <div>D</div>
	<div>REVISION</div> <div>4.0.0</div>		
<div>NOTICE OF PROPRIETARY PROPERTY:</div> <div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:</div> <div>I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE</div> <div>II NOT TO REPRODUCE OR COPY IT</div> <div>III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART</div> <div>IV ALL RIGHTS RESERVED</div>		<div>BRANCH</div> <div>evt-1</div>	
		<div>PAGE</div> <div>125 OF 500</div>	
		<div>SHEET</div> <div>84 OF 98</div>	

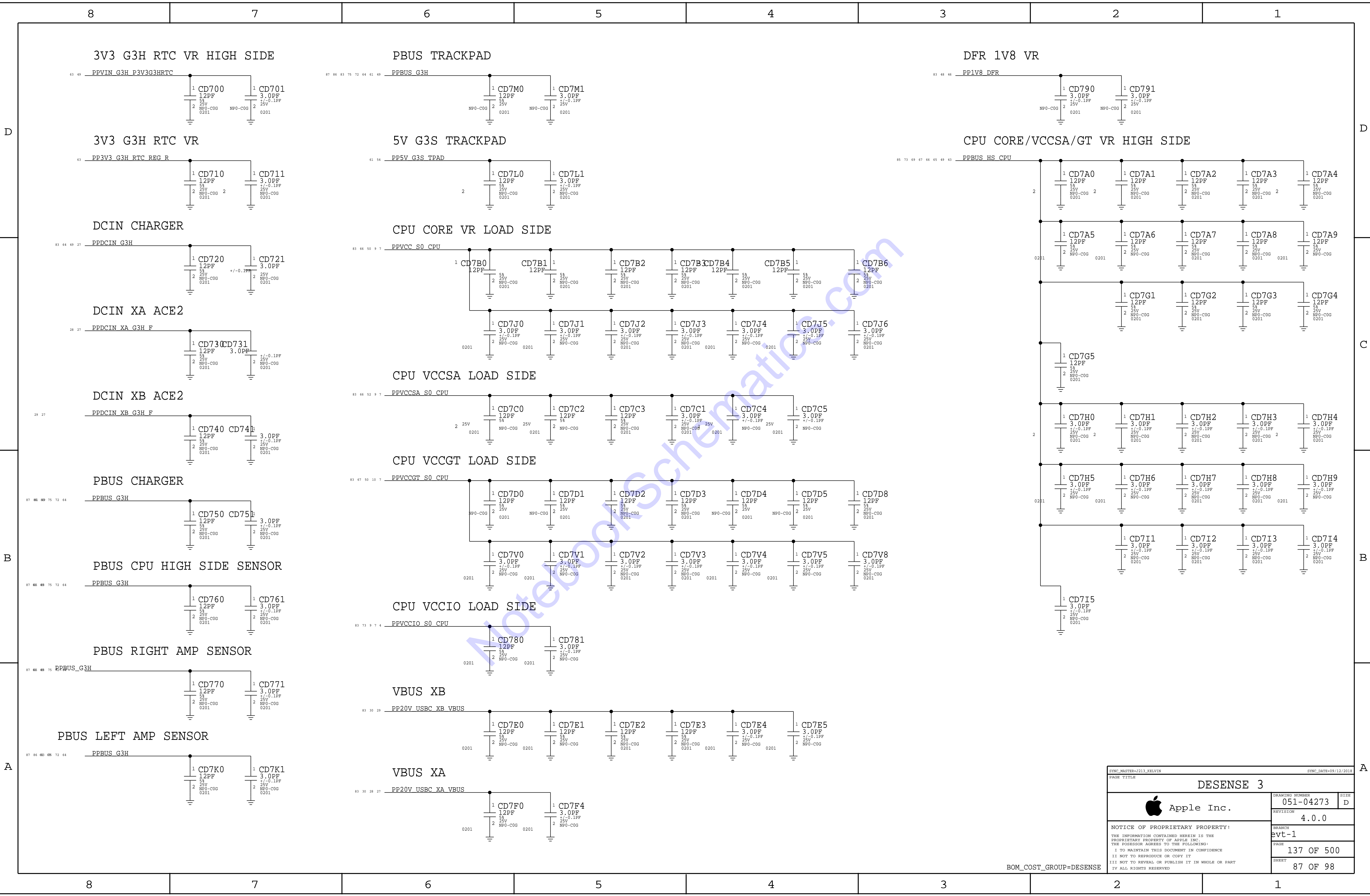



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SYMC_DATE=09/13/2018

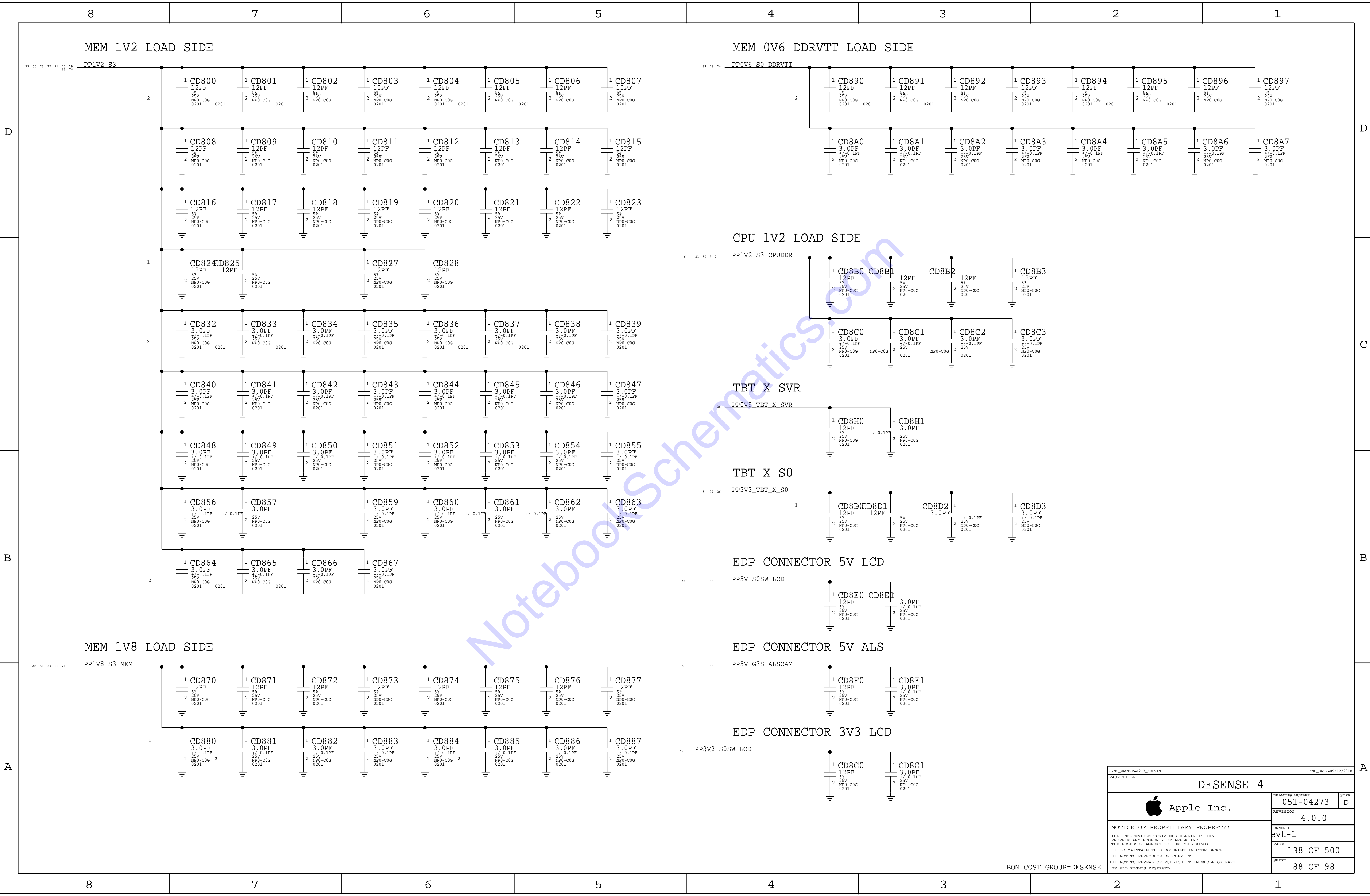
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			BRANCH			evt-1		
			PAGE			136 OF 500		
			SHEET			86 OF 98		
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BOM_COST_GROUP=DESENSE



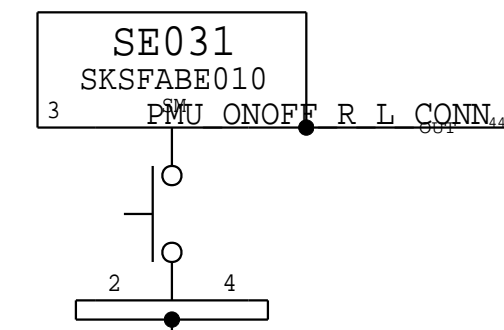
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			PAGE	137 OF 500	
			SHEET	87 OF 98	

BOM_COST_GROUP=DESENSE

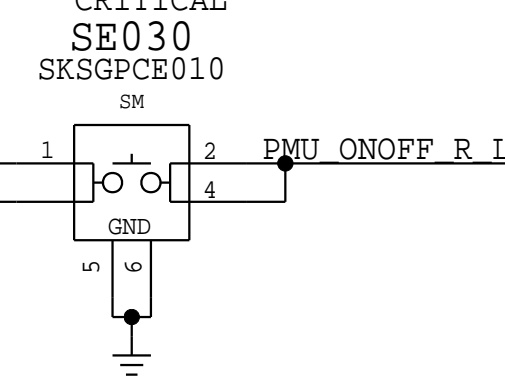


Debug Power "Buttons"

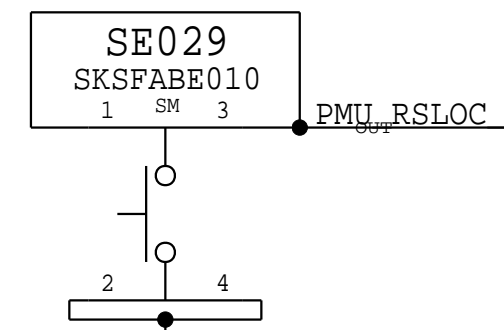
DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=PWR_BTN
CRITICAL



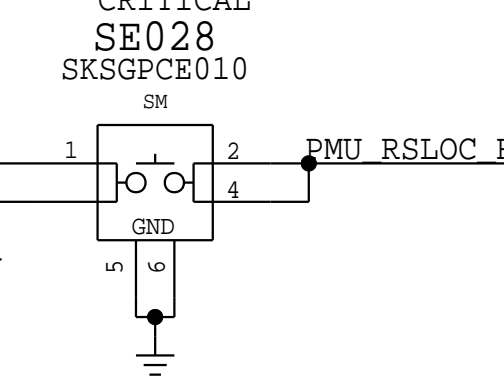
DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=RSLOC
CRITICAL



DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=FORCE_DFU
CRITICAL

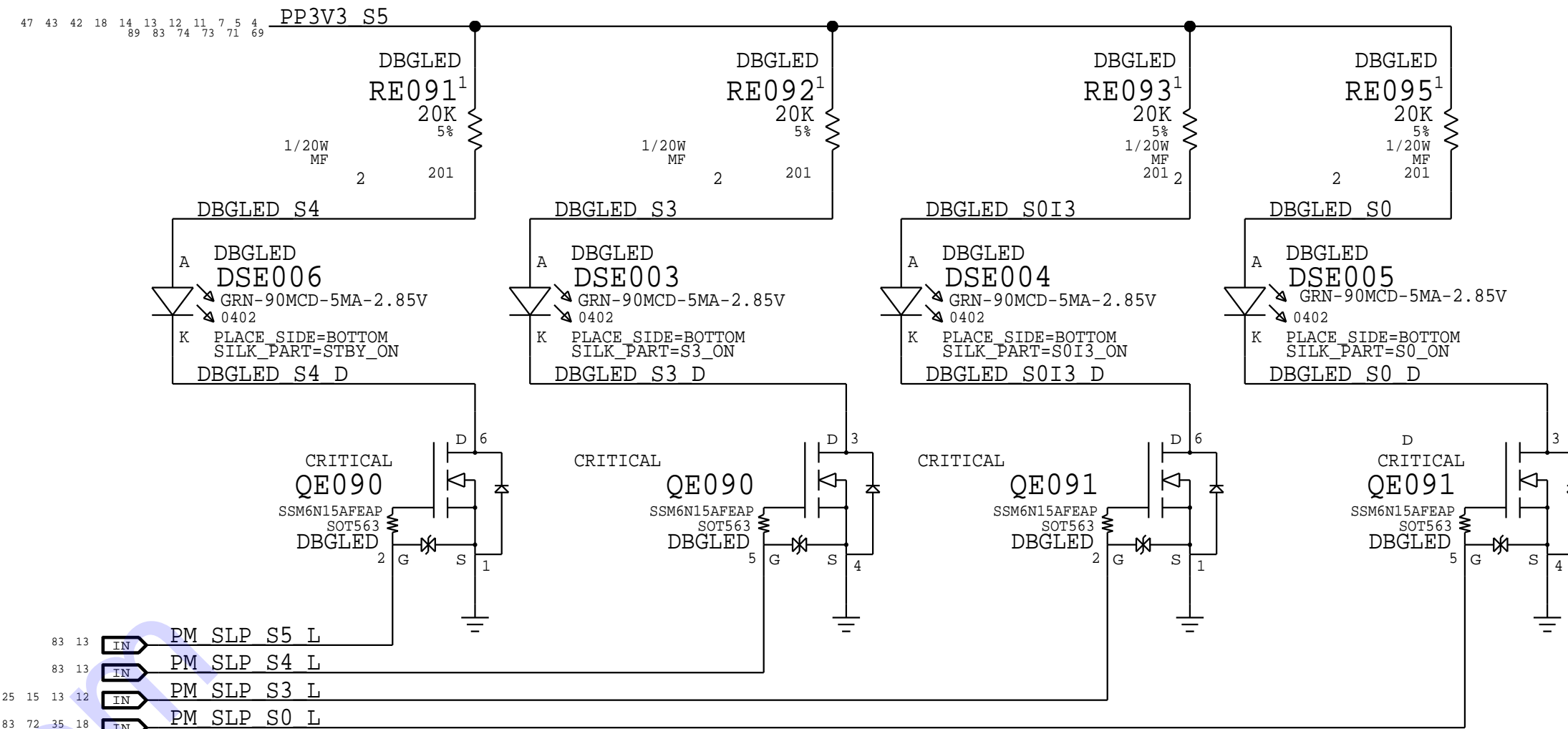


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CRITICAL



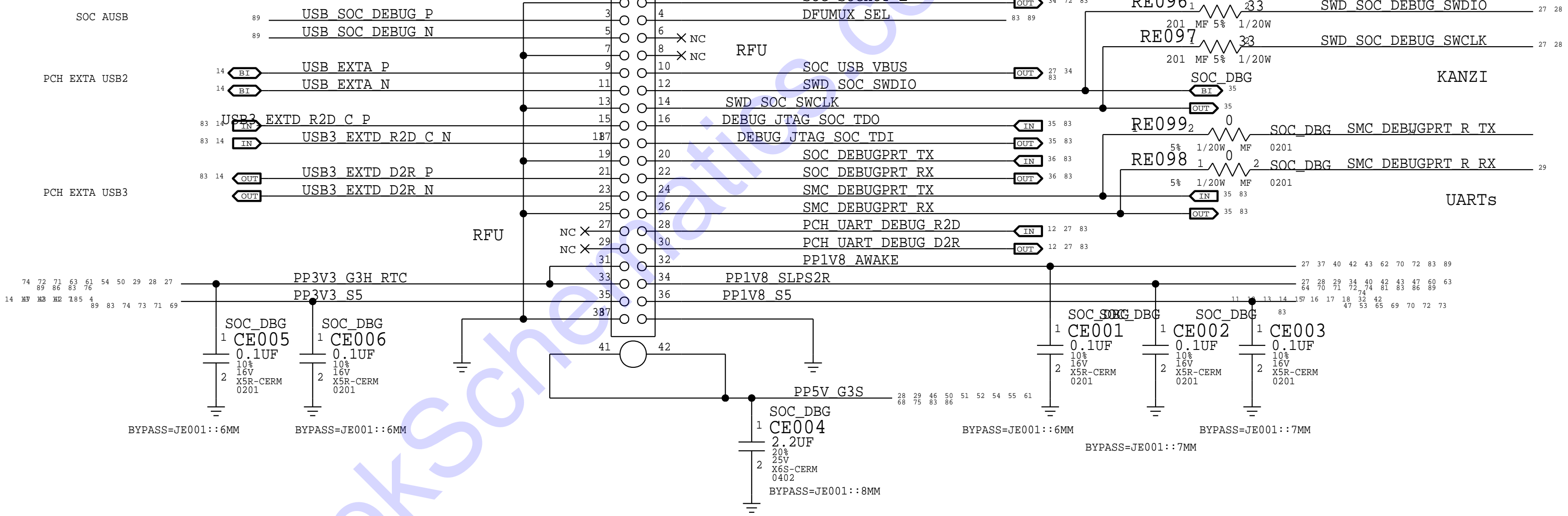
Power State Debug LEDs

(For development only)

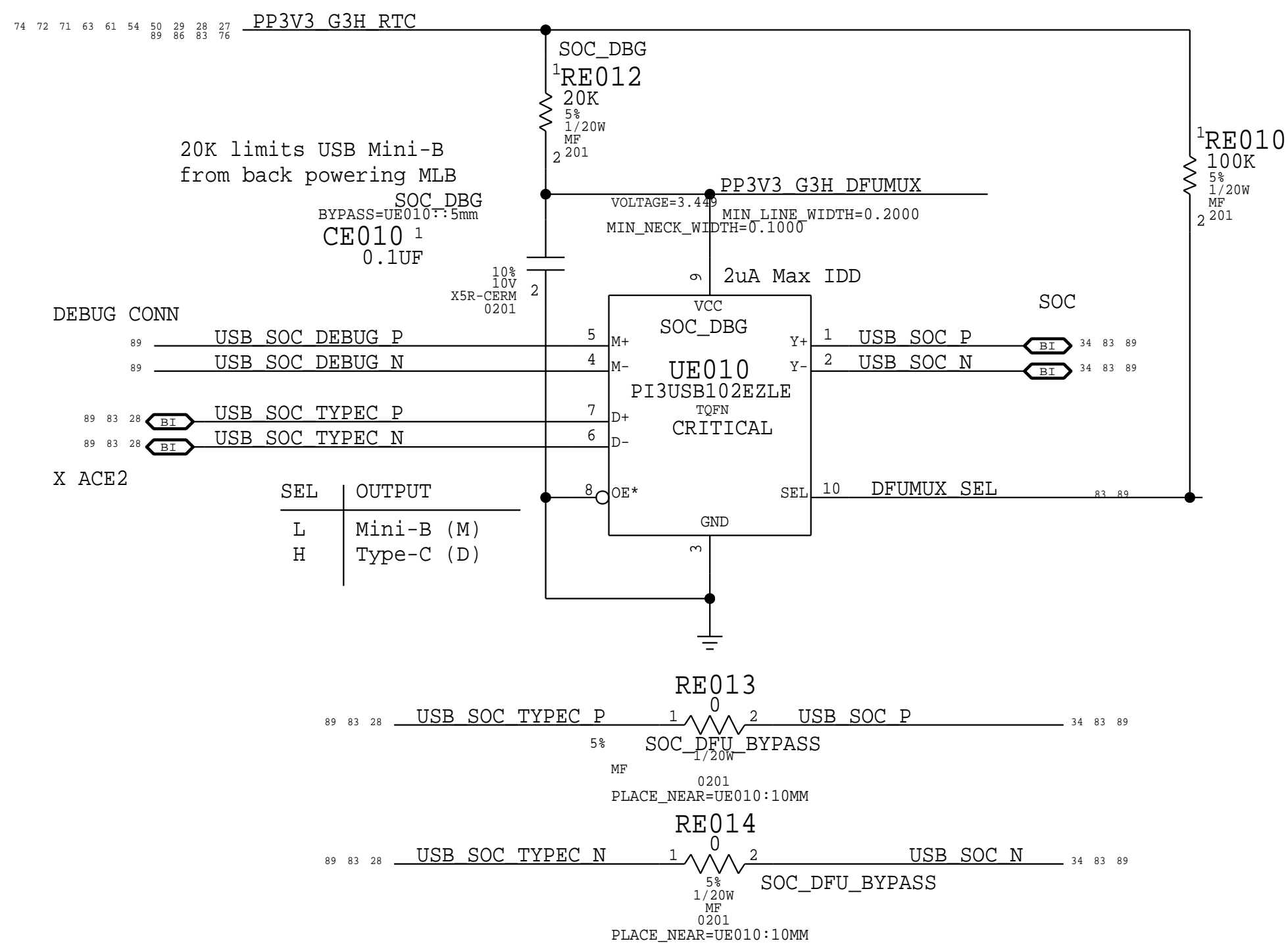


SOC Debug Connector

51681074
SILK_PART=SOC_DBG
SOC_DBG
JE001
AA25D-S038VA1

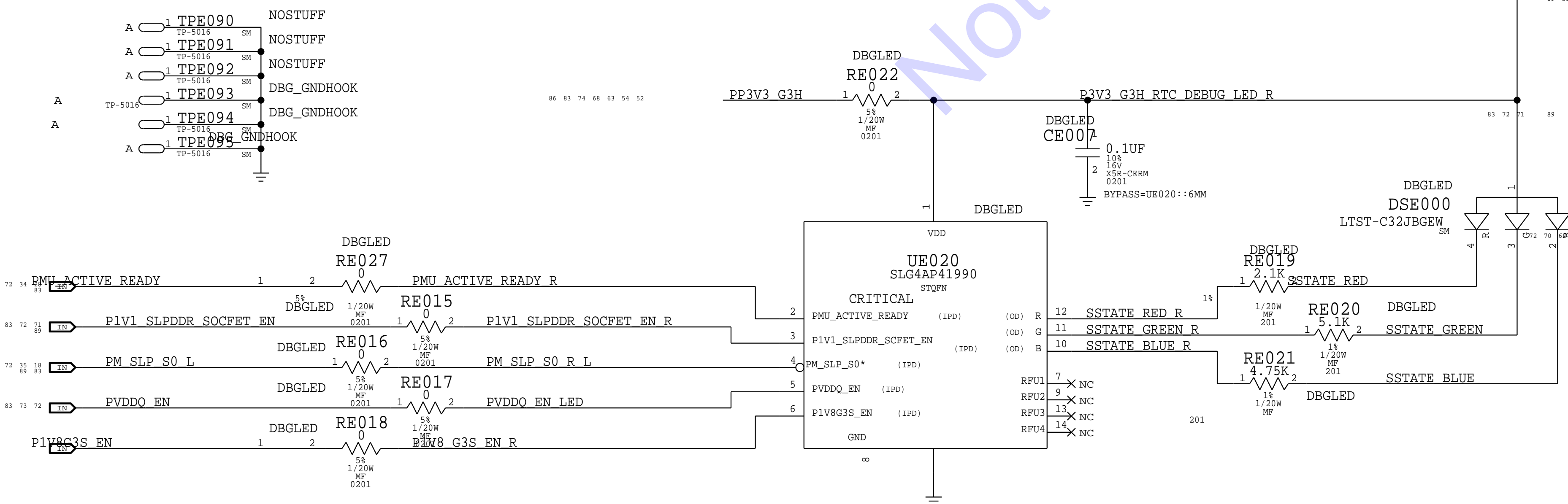


SoC USB DFU Mux

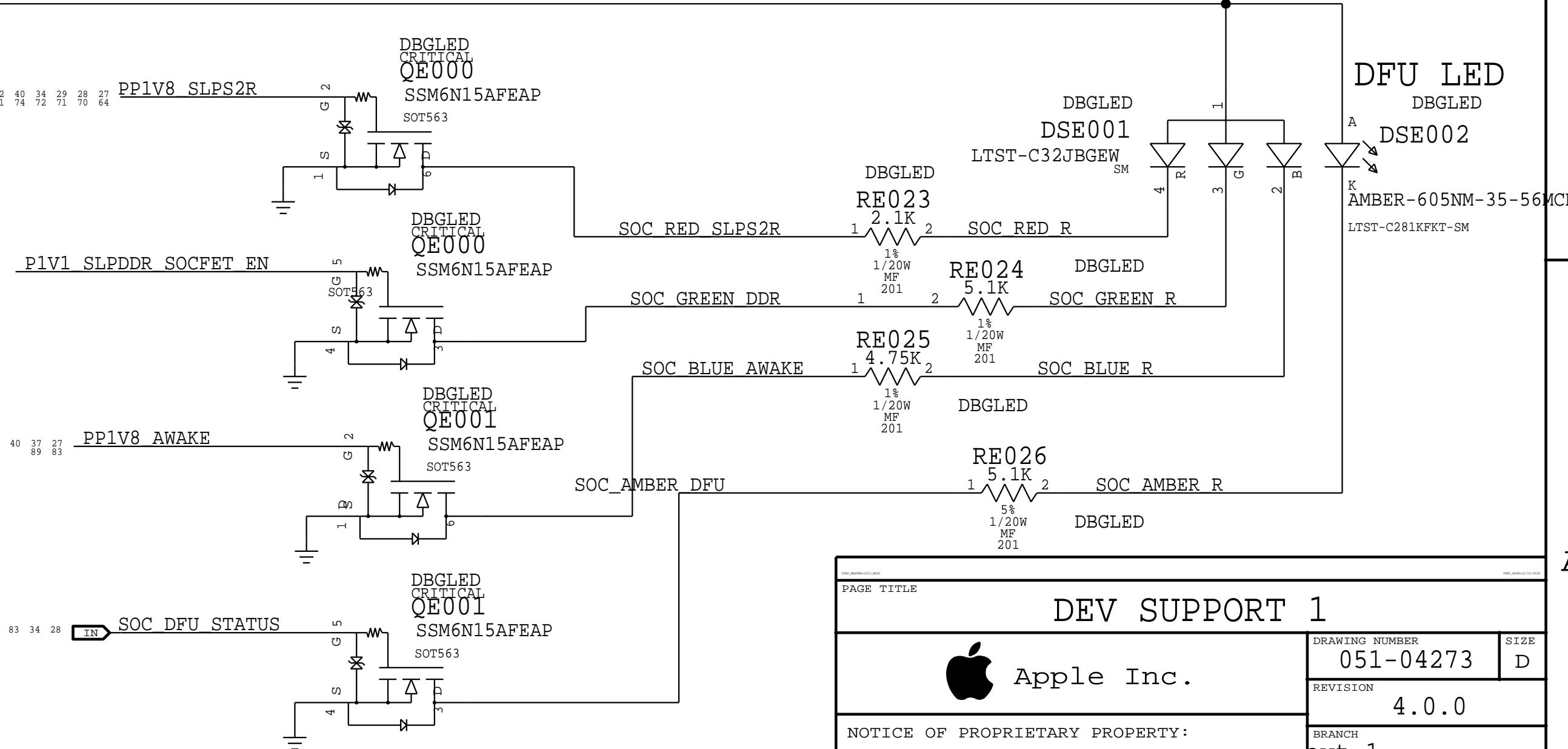


System State LEDs

See color table on next page



SOC State LEDs



PAGE TITLE		
DEV SUPPORT 1		
	DRAWING NUMBER	051-04273
	REVISION	4.0.0
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	PAGE	140 OF 500
SHEET		89 OF 98

BOM_COST_GROUP=DEBUG

8		7		6		
COMMON BOM GROUPS						
BOM GROUP		BOM OPTIONS				
X1536_COMMON_PARTS		SCH,PCB,ALT_CMN,COMMON,ALTERNATE:PART,X1536_USB,X1536_WIRELESS,X1536_X86,X1536_MISC,X1536_T290				
X1536_USB		TBT:TR_C1_PRQ,UPC:ACE2_B2,TBT_ROM:EVT				
1536_WIRELESS	MODULE:MUR_ES_3P1,WIFI_ROM:V00,BT_ROM:P1					
X1536_X86	EDP_ENABLE,DR_MOS_CORE:VISHAY,DR_MOS_VCCSA:VISHAY,DR_MOS_GT:VISHAY,IND_VCCSA:CYNTEC					
X1536_T290		BOARDID3,BOARDID4,BOOTCFG0,BOARDREV1,CALPE_L:OTP_BC,SE:ES2P1_PROD,NAND_VCC:2.5V				
X1536_MISC		CHARGER_IC:POC,AMR:POC,BMU_FLEX:POC,SPEAKER_AMP:C0				

DEBUG BOM PARTS

BOM GROUP	BOM OPTIONS
X1536_DEV_1	ALT_CMN, ALTERNATE:PART,DBGLED,DBG_FAN,DEBUG_BUTTON,ESP_I_DBG,SENSOR:DEV,XDP:YES,XDP_CONN:YES
X1536_DEV_2	SSD_DBG,LOADISNS,LOADRC:YES,USBC_AARDVARKANOID,USBC_ARKANOID,SOC_DBG,DBG_GNDHOOK,WIFI_DBG

DRAM AND SPD

BOM GROUP	BOM OPTIONS
X1536_08GB_HY	DRAM:08GB_HY,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L
X1536_08GB_MI	DRAM:08GB_MI,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L
X1536_08GB_SS	DRAM:08GB_SS,RAMCFG3_L,RAMCFG2_L,RAMCFG0_L
X1536_16GB_HY	DRAM:16GB_HY,RAMCFG4_L,RAMCFG3_L,RAMCFG1_L,RAMCFG0_L
X1536_16GB_MI	DRAM:16GB_MI,RAMCFG4_L,RAMCFG3_L,RAMCFG1_L
X1536_16GB_SS	DRAM:16GB_SS,RAMCFG3_L,RAMCFG0_L
X1536_NO_DRAM	DRAM:OFF

CPU

BOM GROUP	BOM OPTIONS
X1536_CPU_1P4GHZ	CPU:15W_1P4G_QRH7
X1536_CPU_1P7GHZ	CPU:15W_1P7G_QRH6
X1536_CPU_NO_CPU	CPU:0OFF

SOC AND NAND

BOM GROUP	BOM OPTIONS
X1536_TLC_128GB_HY	SOC:PROD_B0_1G,SSD:2L,NAND_U8600:2DP_HY,NAND_U8700:2DP_HY
X1536_TLC_128GB_TS	SOC:PROD_B0_1G,SSD:2L,NAND_U8600:2DP_TS,NAND_U8700:2DP_TS
X1536_TLC_256GB_HY	SOC:PROD_B0_1G,SSD:4L,NAND_U8600:4DP_HY,NAND_U8700:2DP_HY,NAND_U8800:2DP_HY,NAND_U8900:2DP_HY
X1536_TLC_256GB_TS	SOC:PROD_B0_1G,SSD:4L,NAND_U8600:4DP_TS,NAND_U8700:2DP_TS,NAND_U8800:2DP_TS,NAND_U8900:2DP_TS
X1536_TLC_256GB_SS	SOC:PROD_B0_1G,SSD:4L,NAND_U8600:4DP_SS,NAND_U8700:2DP_SS,NAND_U8800:2DP_SS,NAND_U8900:2DP_SS
X1536_TLC_512GB_HY	SOC:PROD_B0_1G,SSD:4L,NAND_U8600:6DP_HY,NAND_U8700:6DP_HY,NAND_U8800:4DP_HY,NAND_U8900:4DP_HY
X1536_TLC_512GB_TS	SOC:PROD_B0_1G,SSD:4L,NAND_U8600:6DP_TS,NAND_U8700:6DP_TS,NAND_U8800:4DP_TS,NAND_U8900:4DP_TS
X1536_TLC_001TB_HY	SOC:PROD_B0_2G,SSD:4L,NAND_U8600:10DP_HY,NAND_U8700:10DP_HY,NAND_U8800:8DP_HY,NAND_U8900:8DP_HY
X1536_TLC_001TB_TS	SOC:PROD_B0_2G,SSD:4L,NAND_U8600:10DP_TS,NAND_U8700:10DP_TS,NAND_U8800:8DP_TS,NAND_U8900:8DP_TS
X1536_TLC_002TB_HY	SOC:PROD_B0_2G,SSD:4L,NAND_U8600:16DP_HY,NAND_U8700:16DP_HY,NAND_U8800:16DP_HY,NAND_U8900:16DP_HY
X1536_TLC_002TB_WD	SOC:PROD_B0_2G,SSD:4L,NAND_U8600:16DP_WD,NAND_U8700:16DP_WD,NAND_U8800:16DP_WD,NAND_U8900:16DP_WD
X1536_NO_NAND_2_LD	SOC:PROD_B0_2G,SSD:2L,NAND_U8600:OFF,NAND_U8700:OFF,NAND_U8800:OFF,NAND_U8900:OFF
X1536_NO_NAND_4_LD	SOC:PROD_B0_2G,SSD:4L,NAND_U8600:OFF,NAND_U8700:OFF,NAND_U8800:OFF,NAND_U8900:OFF

CPU DRAM CFG[4:0] CHART

	DIE REV	CFG 4	
	A	0	
B		1	
	SPEED	CFG 3	
	2133	0	
	1866	1	

	VENDOR	CFG 1	CFG 0
	HYNIX	0	0
	MICRON	0	
	SAMSUNG	1 0	
	N/A	1	1

	CAPACITY	CFG 2
GB		0
	16GB	1

SYSTEM PARTS

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
	051-04273	1	SCHEM,MLB COFFEE,X1536	SCH	CRITICAL	SCH
	820-01598	1	PCBF,MLB COFFEE,X1536	PCB	CRITICAL	PCB
	685-00257	1	COMMON PARTS,MLB COFFEE,X1536	COMMON_PARTS	CRITICAL	X1536_COMMON_BOM
985-00796	1	DEV,COMMON PARTS,MLB COFFEE,X1536	DEV_PARTS	CRITICAL		X1536_DEV_BOM

TOP LEVEL BOM

639-XXXX (POR) OR 939-XXXX (DEV)

COMMON PARTS BOM

685-00257

- DEBUG PARTS BOM

985-00796

COMMON PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00257	COMMON_PARTS,MLB COFFEE,X1536	X1536_COMMON_PARTS

DEBUG PARTS

	BOM NUMBER	BOM NAME	BOM OPTIONS
985-00796		DEV,COMMON_PARTS,MLB COFFEE,X1536	X1536_DEV_1,X1536_DEV_2

NOTES :


"SENSOR:DEV" IS FOR SENSE RESISTORS. WHEN CURRENT SENSING IS REMOVED AT DVT, THESE RESISTORS WILL BE REPLACED WITH A SPECIAL SYMBOL, A COPPER SHAPE SHORTING THE TWO TERMINALS

"LOADISNS" ARE CIRCUITS ONLY REQUIRED UNTIL DVT TO MEASURE/SENSE CURRENT. SENSE CIRCUITS REQUIRED BY SMC WILL NOT HAVE THIS OPTION SINCE THEY WILL STAY TILL PVT

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*LOADRC:YES/NO* RC FILTERS INTO ADC WILL BE REPLACED BY 100K PD ONCE THE SENSE CIRCUITS GO
AWAY

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SYNC_MASTER=J213 JOHN		SYNC_DATE=06/05/2018	
PAGE TITLE			
BOM GROUPS			
 Apple Inc.	DRAWING NUMBER 051-04273		SIZE D
	REVISION 4.0.0		
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	8	7	6	5	4	3	2	1										
D	<div>DEV BOMS - NO CPU, NO DRAM, NO SSD</div> <table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>939-07159</td><td>DEV,MLB,NO-CPU-MEM-NAND,2-LAND,X1536</td><td>ALT_OWN,ALTERNATE:PART,X1536_COMMON_BOM,X1536_DEV_BOM,X1536_CPU_M0_CPU,X1536_M0_DRAM,X1536_M0_NAND_2_LD</td></tr><tr><td>939-07160</td><td>DEV,MLB,NO-CPU-MEM-NAND,4-LAND,X1536</td><td>ALT_OWN,ALTERNATE:PART,X1536_COMMON_BOM,X1536_DEV_BOM,X1536_CPU_M0_CPU,X1536_M0_DRAM,X1536_M0_NAND_4_LD</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	939-07159	DEV,MLB,NO-CPU-MEM-NAND,2-LAND,X1536	ALT_OWN,ALTERNATE:PART,X1536_COMMON_BOM,X1536_DEV_BOM,X1536_CPU_M0_CPU,X1536_M0_DRAM,X1536_M0_NAND_2_LD	939-07160	DEV,MLB,NO-CPU-MEM-NAND,4-LAND,X1536	ALT_OWN,ALTERNATE:PART,X1536_COMMON_BOM,X1536_DEV_BOM,X1536_CPU_M0_CPU,X1536_M0_DRAM,X1536_M0_NAND_4_LD	D
BOM NUMBER	BOM NAME	BOM OPTIONS																
939-07159	DEV,MLB,NO-CPU-MEM-NAND,2-LAND,X1536	ALT_OWN,ALTERNATE:PART,X1536_COMMON_BOM,X1536_DEV_BOM,X1536_CPU_M0_CPU,X1536_M0_DRAM,X1536_M0_NAND_2_LD																
939-07160	DEV,MLB,NO-CPU-MEM-NAND,4-LAND,X1536	ALT_OWN,ALTERNATE:PART,X1536_COMMON_BOM,X1536_DEV_BOM,X1536_CPU_M0_CPU,X1536_M0_DRAM,X1536_M0_NAND_4_LD																
									C									
B									B									
A									A									
	8	7	6	5	4	3	2	1										

SYNC_MASTER=J213_JOHN

SYNC_DATE=06/05/2018

PAGE TITLE

BOM VARIANT TABLES

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DRAWING NUMBER

051-04273

REVISION

4.0.0

BRANCH

evt-1

PAGE

407 OF 500

SHEET

96 OF 98

SIZE

D

RULER_RULE_SET=RIGID_2016		MANUFACTURING CONFIGURATION			TABLE_REV_NUMBER=1	
DIELECTRIC BASED SPACING RULES				DEFAULT SPACING MULTIPLES	VOID SPACE RATIO	
MULTIPLES	SMDPIN MAX(UM)	UVIA MAX(UM)	SMDPIN2SMDPIN MAX(UM)			
1,2,3,4,5,6,7,8,9,10,11,12,13,14	120	120	100	1	2	
LAYERS		MINIMUM CU WIDTH RATIO	MINIMUM CU SPACING RATIO	MINIMUM TO DEFAULT RATIO		
TOP,BOTTOM		2.0	2.36842	1.2		
ISL2,ISL13		2.25	2.5	1.2		
ISL3,ISL12		2.0	2.25806	1.2		
ISL4,ISL11		2.5	2.5	1.2		
ISL5,ISL10		2.5	2.5	1.2		
ISL6,ISL9		2.5	2.5	1.2		
ISL7,ISL8		2.0	2.25806	1.2		

MANUAL EDITS AFTER AUTOGENERATION:

OVERWROTE THROUGH VIA, BB VIA, AND UVIA SPACINGS TO DEFAULT VALUE, THE AUTOGEN ONES ARE TOO HIGH

UPDATE SAME NET SPACING FOR VIA TO HOLE, UVIA TO SMD PIN, FOR DEFAULT AND MIN, TO -1

CHANGED LINE TO SMD SAME NET SPACING FROM 0.1 TO 0.07 ON TOP/BOTTOM LAYERS

CHANGED MAX NECK LENGTH FOR THE DEFAULT PHYSICAL RULE TO 20MM

CHANGED UVIA TO LINE SAME NET SPACING TO 0.05

CHANGED BB VIA TO LINE, ABD BB VIA TO BB VIA SAME NET SPACING TO 0.0

CHANGED BB VIA TO UVIA SAME NET SPACING TO -1

CHANGED LINE TO SHAPE SAME NET SPACING TO 0.05

SET BB VIA STAGGER IN PHYSICAL RULES TO 0.2500 FOR MIN, 0.275 FOR ALL OTHER, FOR LAYERS 3 AND 12

COPIED THE RULES FROM 85 OHM DIFF TO 85 MIN STAGGER

SET ENABLE DRC BY LAYER IN SAME NET SPACING TO TRUE FOR ALL LAYERS

KEEP DEFAULT AS DEFAULT, GENERIC DP AS GENERIC DP

REPLACING ALL SPACINGS EXCEPT LINE TO LINE WITH DEFAULT VALUES

DECREASED NECK GAP FOR DIFF PAIRS TO VALUE FOR GENERIC DP

REASSIGN SPACING AND PHYSICAL REGION RULES AND NET CLASS ASSIGNMENTS

SET UVIA TO SHAPE SAME NET SPACING TO 0.1MM ON TOP/BOTTOM

